2nd

EU-JAPAN DIGITAL WEEK 2026

23 March - 30 March 2026

Tokyo, Japan

The EU-Japan Digital Week is organised as part of the EU-Japan Digital Partnership

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From research to industrial-scale quantum hardware: building manufacturable silicon qubits

Jean-Charles BARBE, CTO of QUOBLY

Our Story

2000-2015
Our Scientific Foundations

Two research paths
- Quantum engineering
- Technology development for charge and spin properties control in silicon transistors

Within 2 internationally-acclaimed RTOs

cnrs cea

2016-2022
Quobly founders pioneer large scale silicon quantum computers

One research team mission oriented towards large scale computing
- World first demonstration of a silicon qubit from 300mm technology
- 15M€ ERC Synergy grant to tackle scientific challenges

2022
Quobly becomes a company

Quobly spins off from CEA-Leti/CNRS

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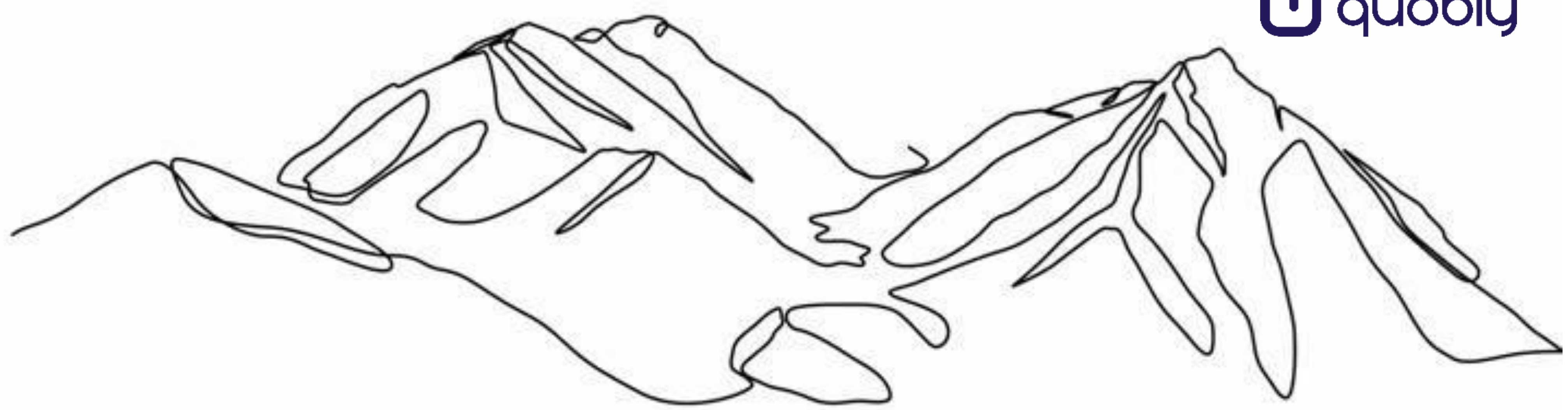

Quobly in 2026

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Large-scale market-driven technology requirements

	Nb of logical qubits		Logical op. frequency			
Material Science & Chemistry	O(100)[1]	+	Frequency 1kHz* *Assuming an answer within 1 day*			(1) Phase Craft materials database
PDEs CFDs	O(100) to O (1000)[2]	+	Frequency 10kHz* *Assuming an answer within 2 hours*			(2) Low, G.H. and Chuang, I.L., (2019). Quantum Simulation of Fluid Dynamics
Optimization	O(1000)[3]	+	Frequency (100kHz)* *Assuming an answer within half an hour*	+	Reasonable costs	(3) Lotshaw, P.C., Nguyen, T., Santana, A. *et al.* Scaling quantum approximate optimization on near-term hardware. *Sci Rep* **12**, 12388 (2022). https://doi.org/10.1038/s41598-022-14767-w

= 1000 logical qubits with logical op freq. between 1kHz & 100kHz to be run for Giga quantum operations

**Assuming 1k shots 10^8 gates*

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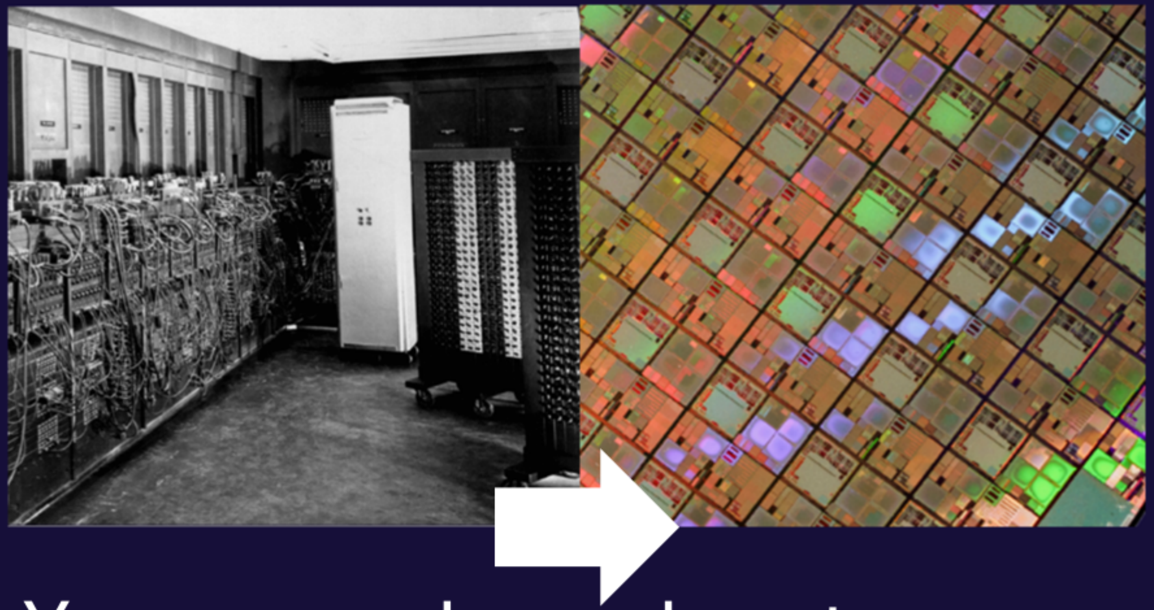
Silicon qubits solve quantum's hardest problems: scalability, size, and cost

- Up to 1M× smaller than other modalities
- Qubits are co-integrated with transistors to scale the control systems
- Million-qubit systems fit in 10 m^2
- QEC relies on surface code and leverages our high qubit count and co-integrated controls
- Leverages existing supply chains and fab infrastructure ($B of CAPEX), built on mature, industrial CMOS technology



You remember valves to transistors?
Our ambition: doing it for quantum!

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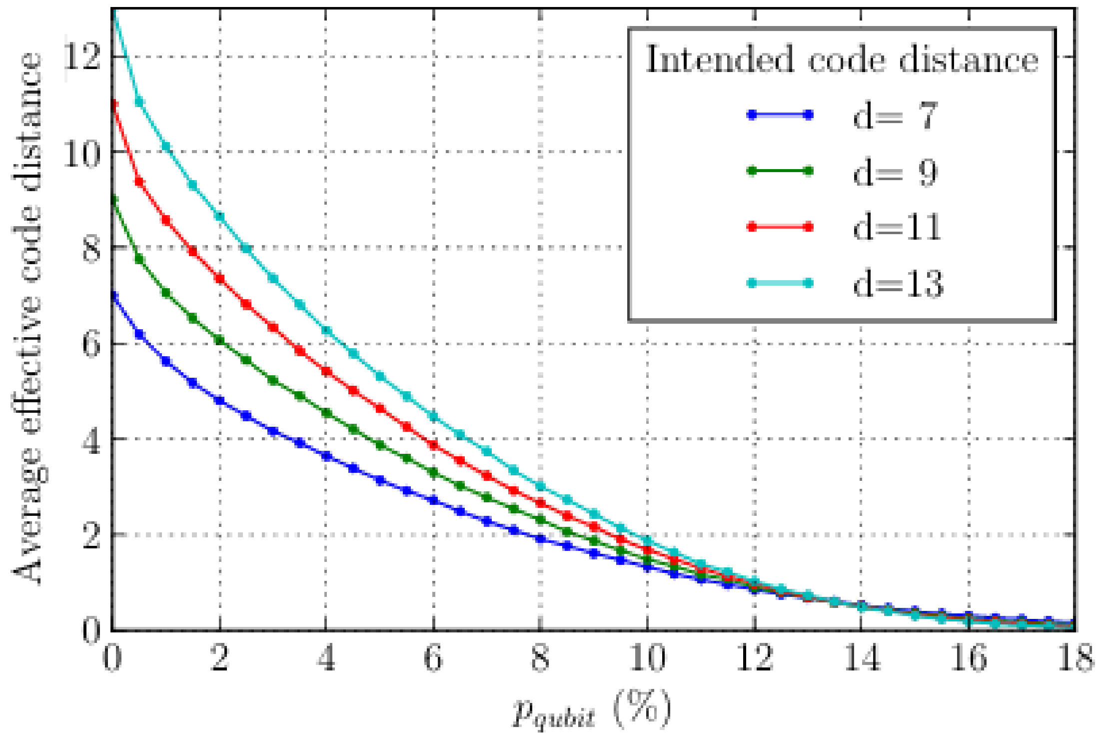
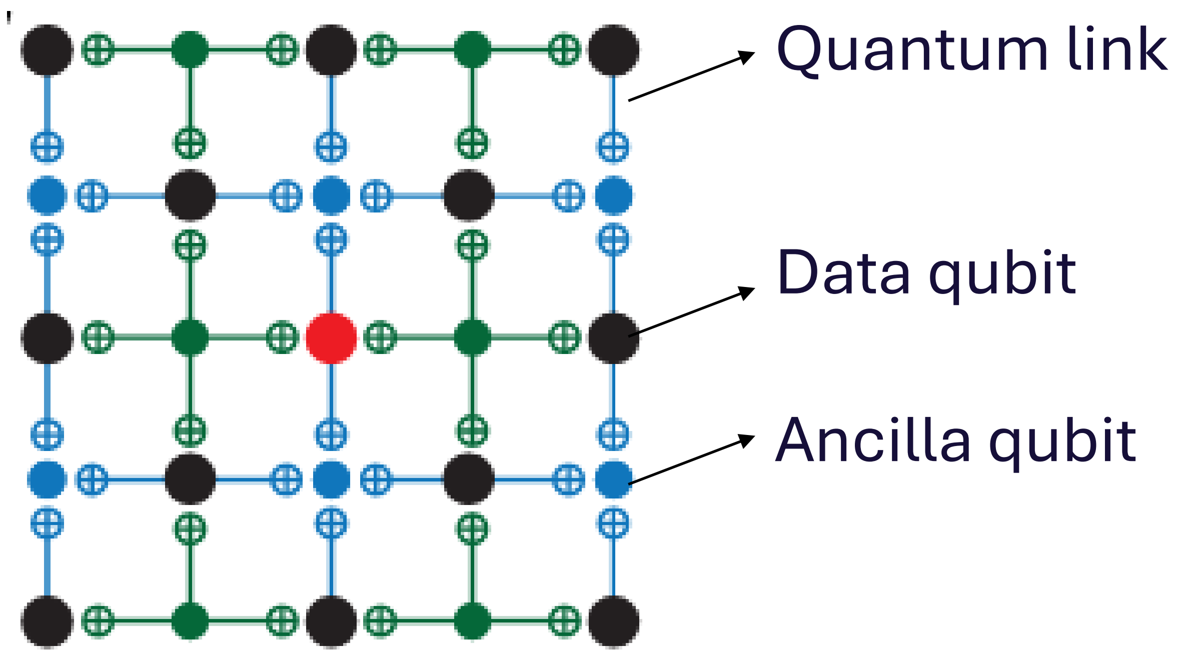
How resilient is surface code on fabrication yield?

Target functionnal qubit yield >99%

Auger and Bandage, PRA 2017





Silicon qubit 2D architecture

Quantum links and qubits are design between 100-1000 electrostatic gates

Targeted fabrication yield for electrostatic gates > 99.999%

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Tech transfer stream applied to quantum bits

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Using tried & tested methods to scale innovations into commercial products

ACADEMIC LABS

1. Demonstrate concept

QuTech, UNSW, CNRS, UCL, TNO, A*

FEW QUBITS

VERSATILE

- Proof of concept
- Quality
- Clock speed

R&D PILOT LINES

2. Explore scalability

Imec, CEA-Leti, Fraunhofer, VTT, A*

MORE QUBITS

INTRODUCTION OF INTEGRATION CONSTRAINTS

- Quality
- Clock speed
- Scalability

COMMERCIAL FABS

3. Industrialize

STMicroelectronics, Intel, Globalfoundries, Infineon

MILLIONS OF QUBITS

HIGH-QUALITY, HIGH-YIELD & REPRODUCIBILITY

- Quality
- Clock speed
- Scalability
- Cost

Commercial fabs are required for quality, yield and reproductibility!

Quobly’s path towards manufacturable qubits

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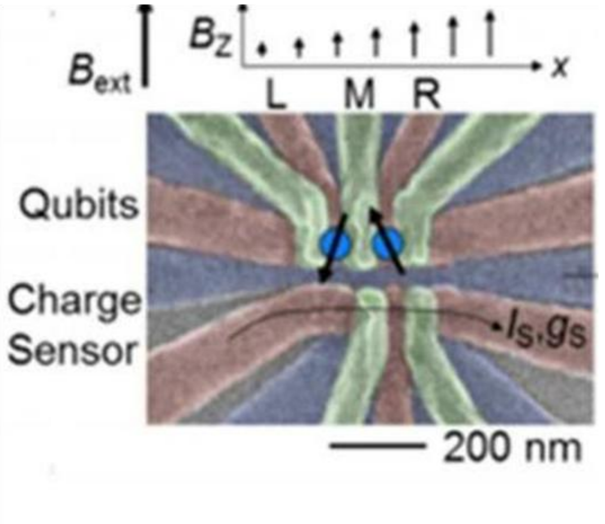
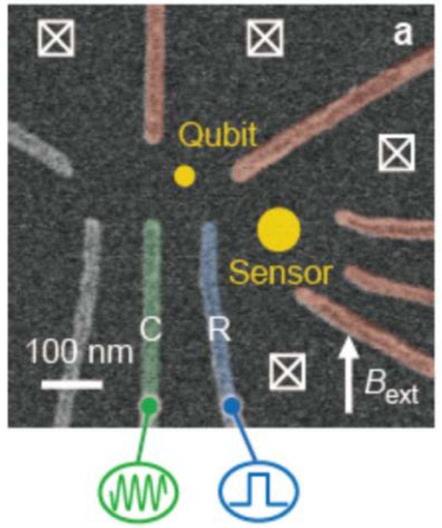
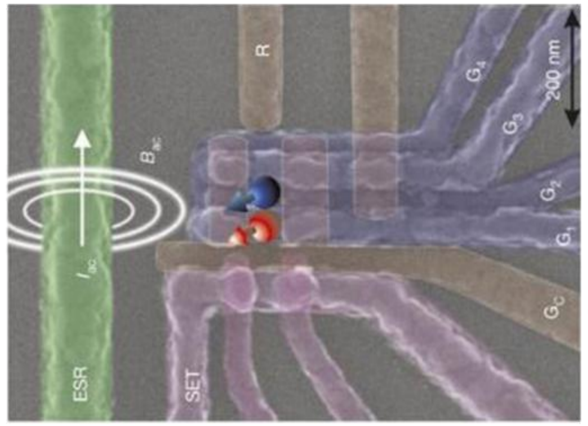
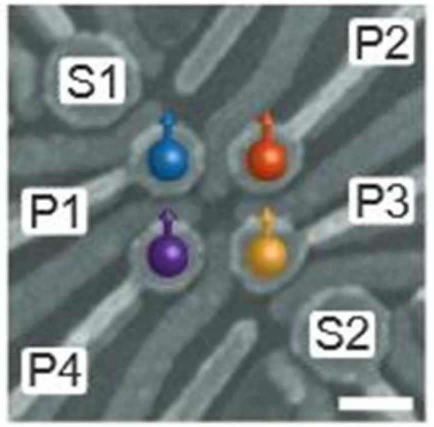
@Princetown, US



@RIKEN, JP



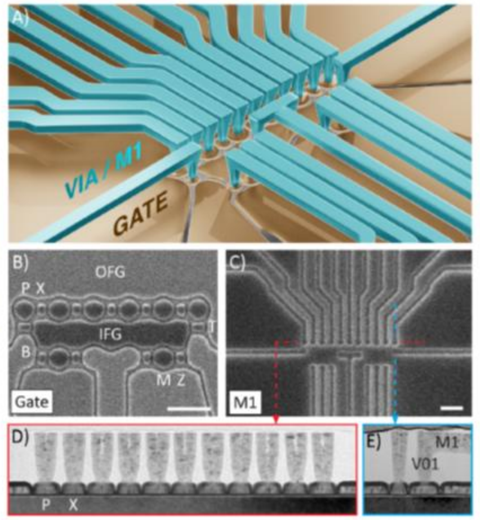




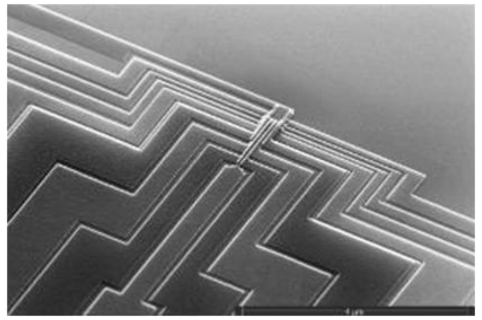
@UNSW, AU

@Delft, NL

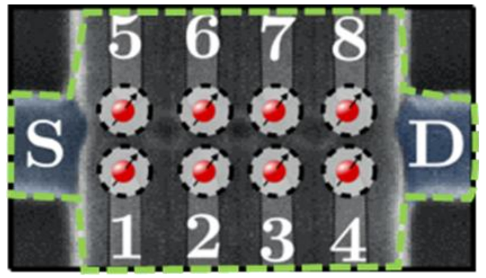
@HRL

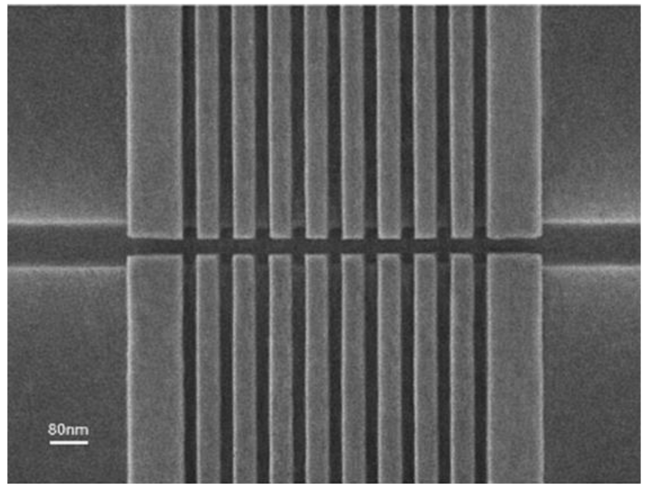


@IMEC



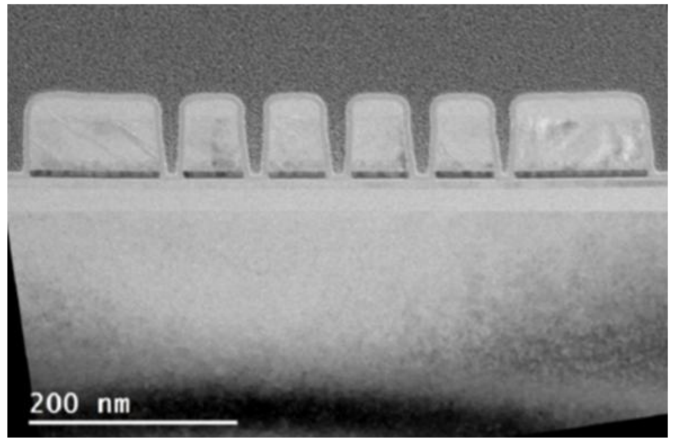
@Grenoble





@Quobly/ST

life.augmented



@Quobly/ST

Academic fab line

Process exploration for qubit performances improvement
Many materials: Si, SiGe, Ge
Many technologies: 2DEG, MOS, FinFET, FD-SOI

R&D pilot lines

300mm wafers
Process robustification to improve qubit performance
Many technologies: 2DEG, MOS, FinFet, FD-SOI

Industrial fab line

300mm wafers
Design and material constrains for high yield
Industrialized technologies: FD-SOI

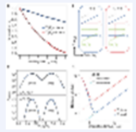
ACADEMIC LABS

Demonstrate concept

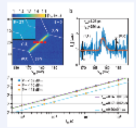
- Proof of concept
- Quality
- Clock speed

Silicon spin qubits have passed the test in academic settings

QUBIT READOUT >99.9 FIDELITY ~µsec

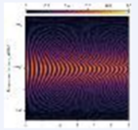


Rapid single-shot parity spin readout in a silicon double quantum dot with fidelity exceeding 99%.
Takeda, K., Noiri, A., Nakajima, T. et al. Quantum Inf (2024)



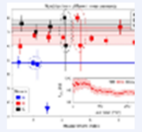
Rapid gate-based spin read-out in silicon using an on-chip resonator.
Zheng, G., Samkharadze, N., Noordam, M.L. et al. Nat. Nanotech. (2019)

1Q UP TO >99.99% FIDELITY 10s-100s nsec

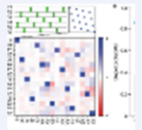


A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%.
Yoneda, J., Takeda, K., Otsuka, T. et al. Nature Nanotech (2018)

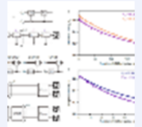
2-QUBIT GATE >99.6% FIDELITY 100s nsec



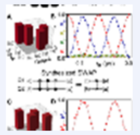
Assessment of the errors of high-fidelity two-qubit gates in silicon quantum dots.
Tanttu, T., Lim, W.H., Huang, J.Y. et al. Nat. Phys. (2024)



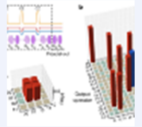
Universal logic with encoded spin qubits in silicon.
Weinstein, A.J., Reed, M.D., Jones, A.M. et al. Nature (2023).



Fast universal quantum gate above the fault-tolerance threshold in Si
Noiri, A., Takeda, K., Nakajima, T. et al. . Nature (2022).

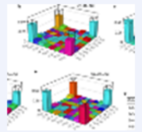


Two-qubit silicon quantum processor with operation fidelity exceeding 99%.
Adam R. Mills et al. Sci. Adv. (2022)

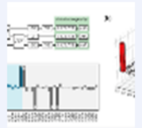


Quantum logic with spin qubits crossing the surface code threshold.
Xue, X., Russ, M., Samkharadze, N. et al. Nature (2022).

3Q ENTANGLEMENT



- Universal control of a six-qubit quantum processor in silicon
- Philips, S.G.J., Mądzik, M.T., Amitonov, S.V. et al. Nature (2022)



- Quantum tomography of an entangled three-qubit state in silicon
- Takeda, K., Noiri, A., Nakajima, T. et al. Nat. Nanotechnol. (2021)

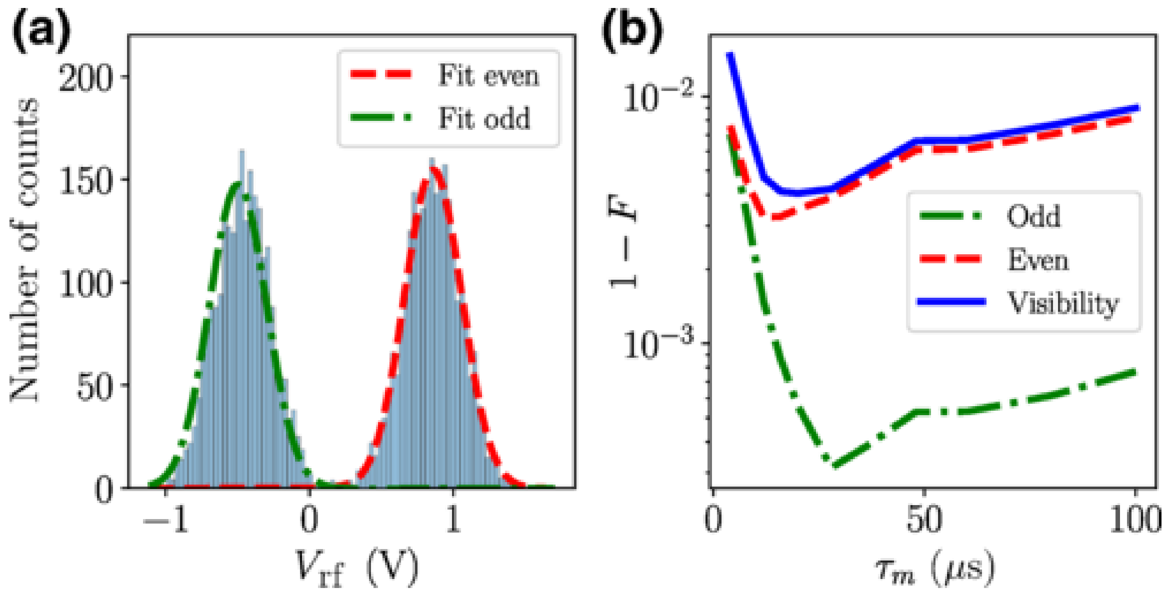
R&D PILOT LINES

Explore scalability

- Quality
- Clock speed
- Scalability

Delivering on speed & quality while respecting strict FD-SOI constraints

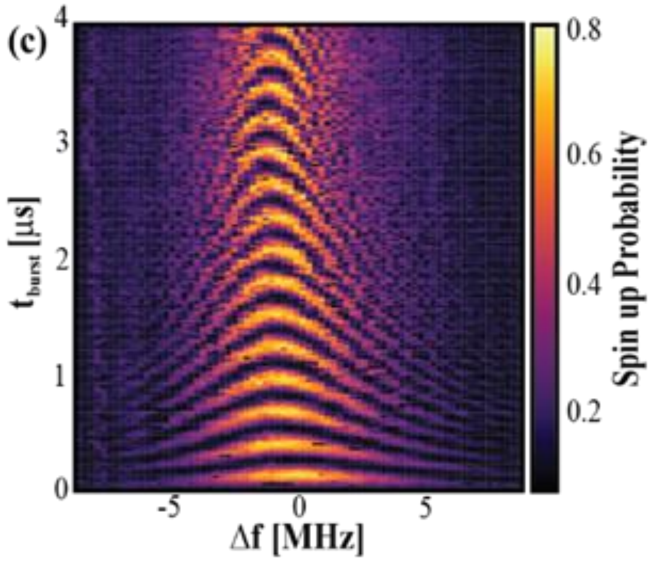
READOUT



>99.93 @ 1 μsec

Urdampilleta et al., Nature Nano 2019
A. Crippa et al., Nature Com 2019
T. Lundberg et al., PRX 2020
D. Niegeman et al., PRX Quantum (2022)
V. El Homsy et al., Arxiv (2023)
B. Cardosa Paz, IEDM 2024

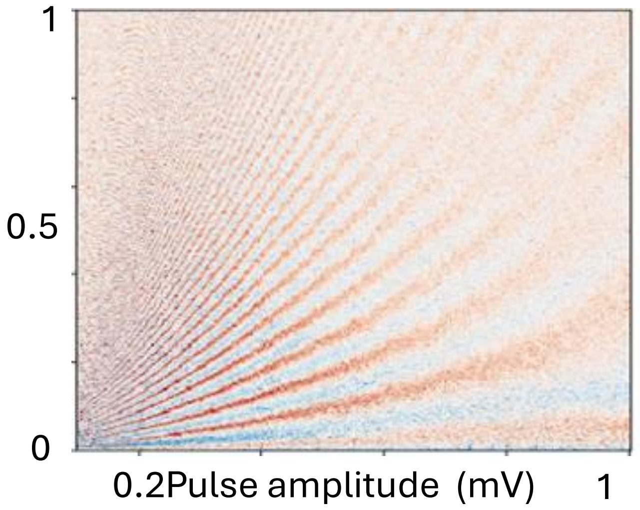
ONE QUBIT GATE



99.6% fidelity 80ns

A. Crippa et al., Nature Com 2019
N. Piot et al., Nature Nano 2022
B. Klemt et al., Nature QI (2023)
B. Paz et al, IEDM 2024

TWO QUBIT GATE



98% fidelity
Record charge noise

P. Hamonic et al, submitted 2024
P. Hamonic et al, in preparation

cea leti
NÉEL institut
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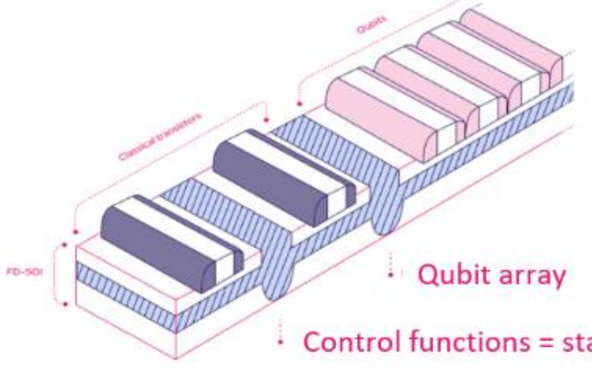
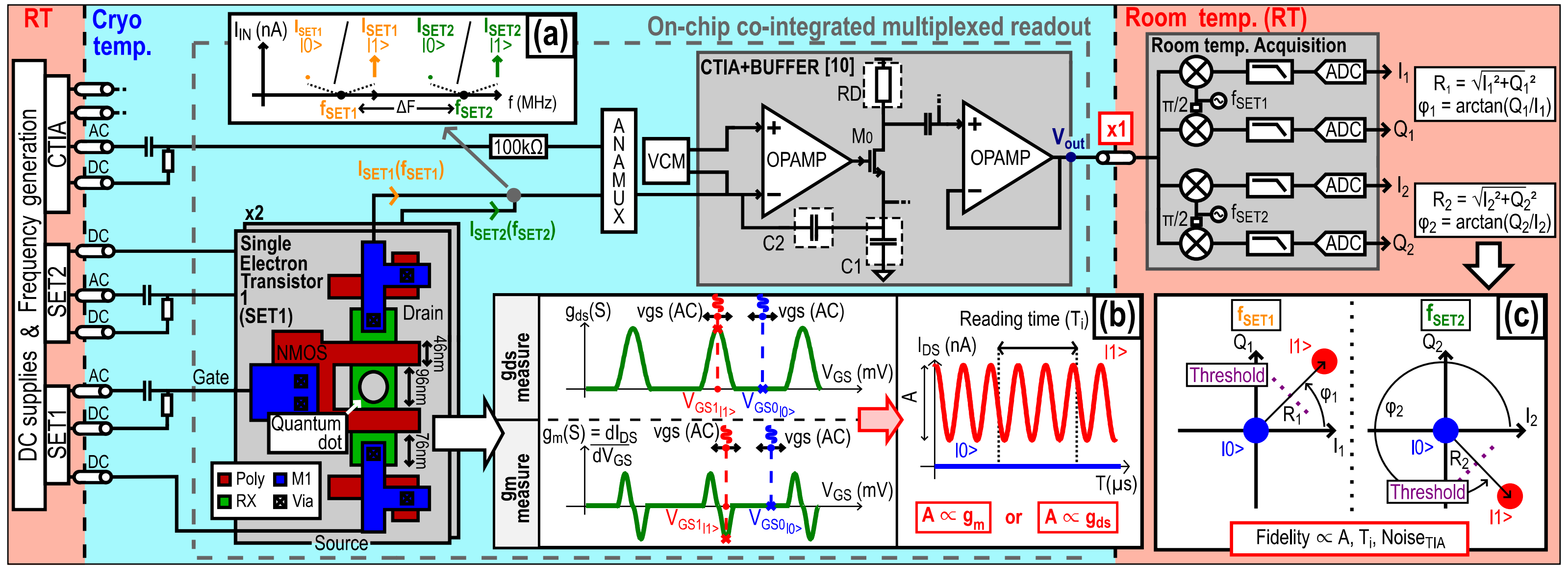
COMMERCIAL FABS
Industrialize
- Quality
- Clock speed
- Scalability
- Cost

Demonstration of co-integration for scalability

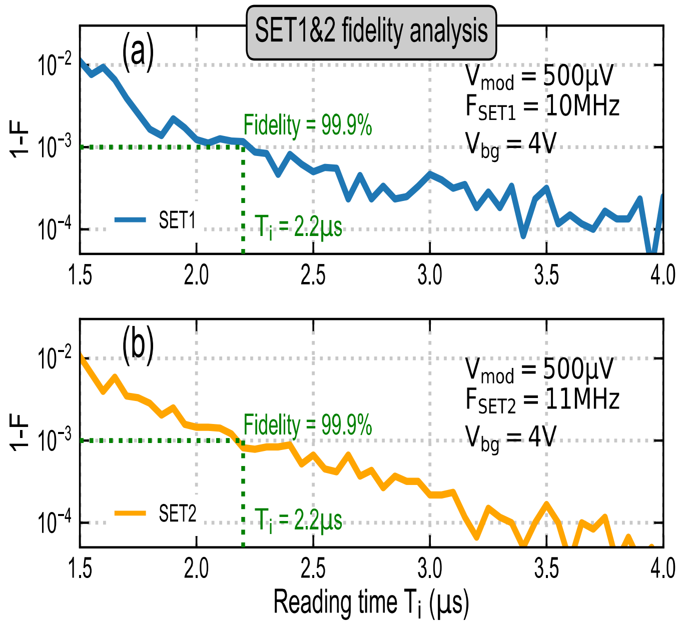


Quantum integrated circuit in cryogenic enviroment

CONTROL ELECTRONICS & QUANTUM DEVICES CO-INTEGRATED AT LOW TEMPERATURE



Q. Schmidt et al., ESSERC 2024



Q. Schmidt et al., ISSCC 2025

In this publication, 1 single wire down to the cryostat to read and control up to 70 qubits

Towards quantum integrated circuit, cryoelectronics for scaling read out

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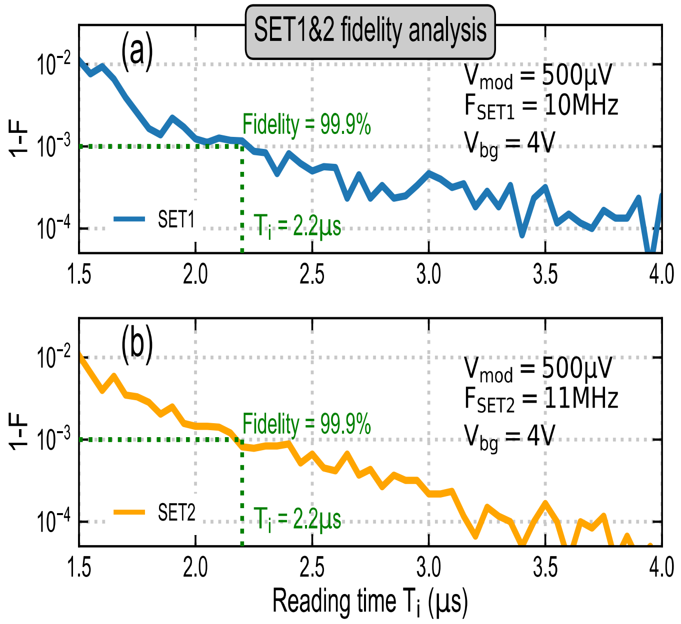
2024

Demonstration of qubit read out multiplexing



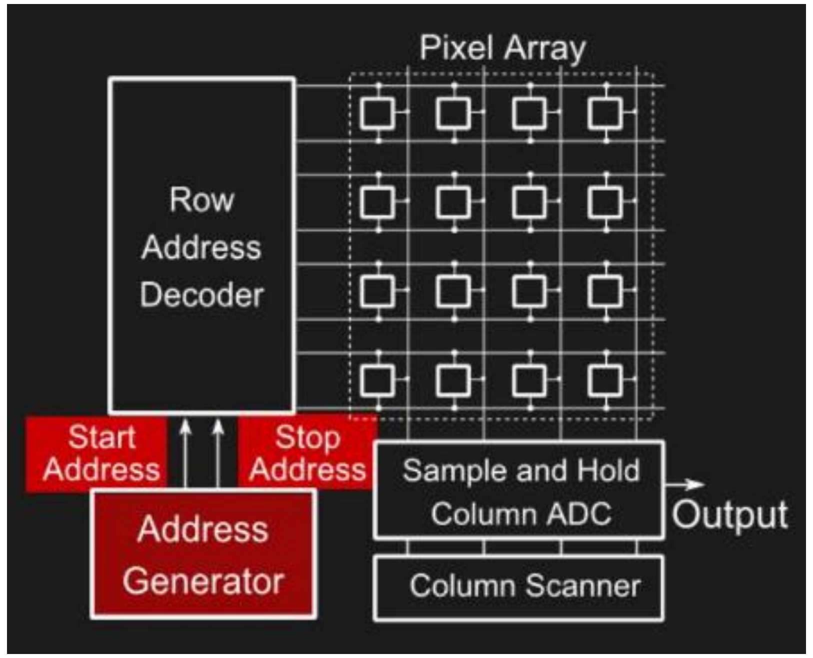
Q. Schmidt et al., ISSCC 2025

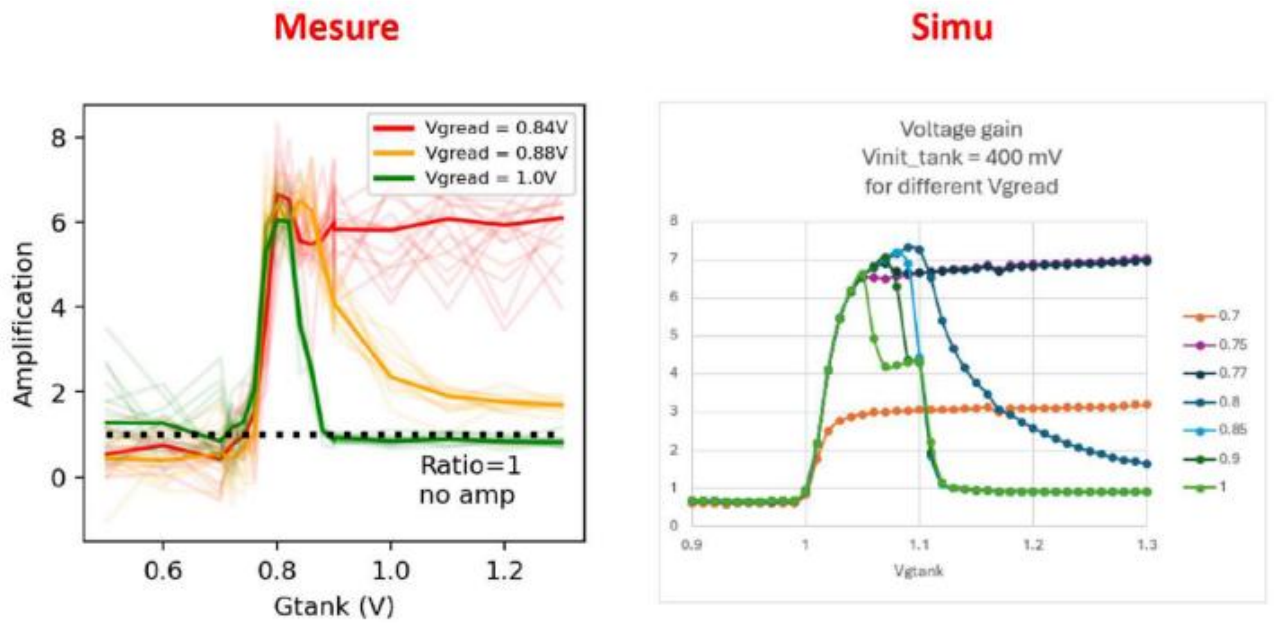
Up to 70 qubits per channel

2025

Adaptation of STMicroelectronics global shutter® CMOS image sensor architecture

20ns to read up 1 million qubits





First HW – model correlation at low temperature for million-qubit architecture

COMMERCIAL FABS
Industrialize
- Quality
- Clock speed
- Scalability
- Cost

High-throughput characterisation capability

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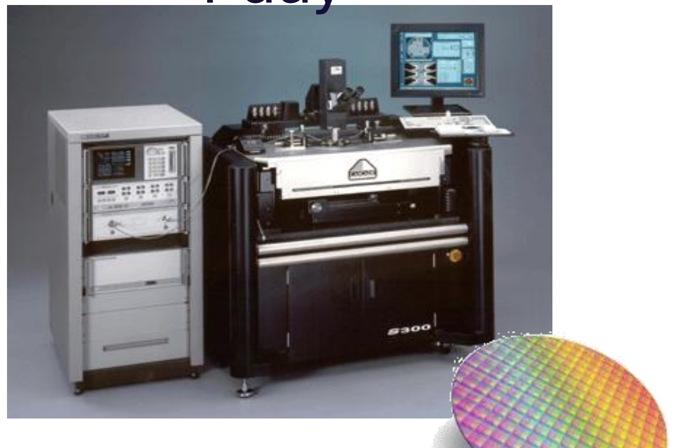
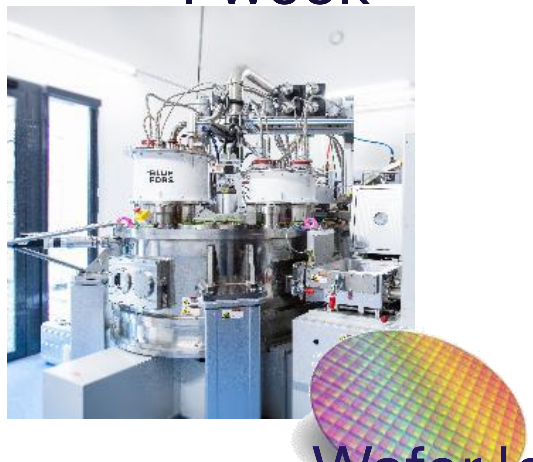
1 day



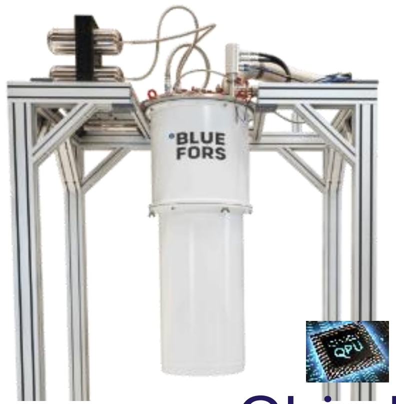
Wafer level

1 week



Wafer level

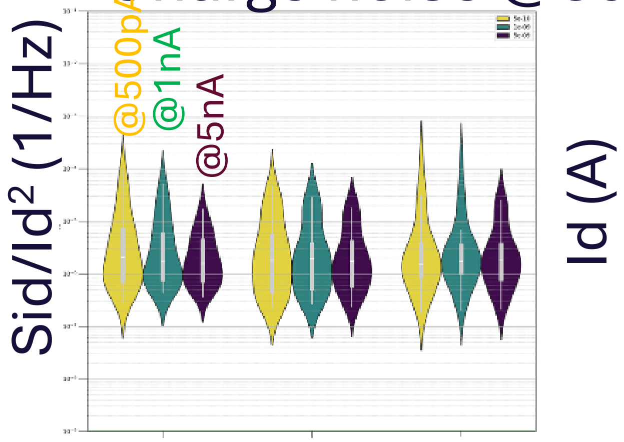
1 month



x2

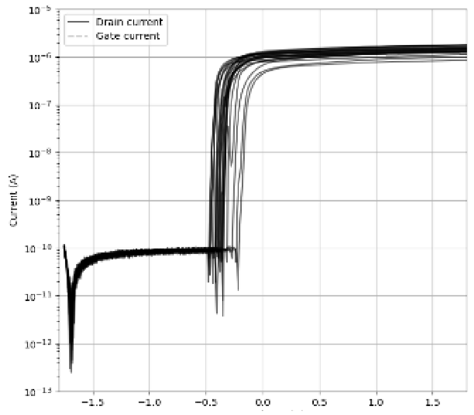
Chip level

Charge noise @300K

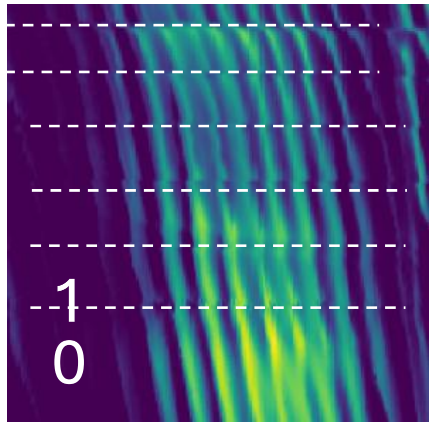


Gate1 Gate2 Gate3

Id-Vg @2K



Gate voltage (V)



Needed to provide integration feedback!

COMMERCIAL FABS

Industrialize

- Quality
- Clock speed
- Scalability
- Cost

High-throughput low temperature characterisation

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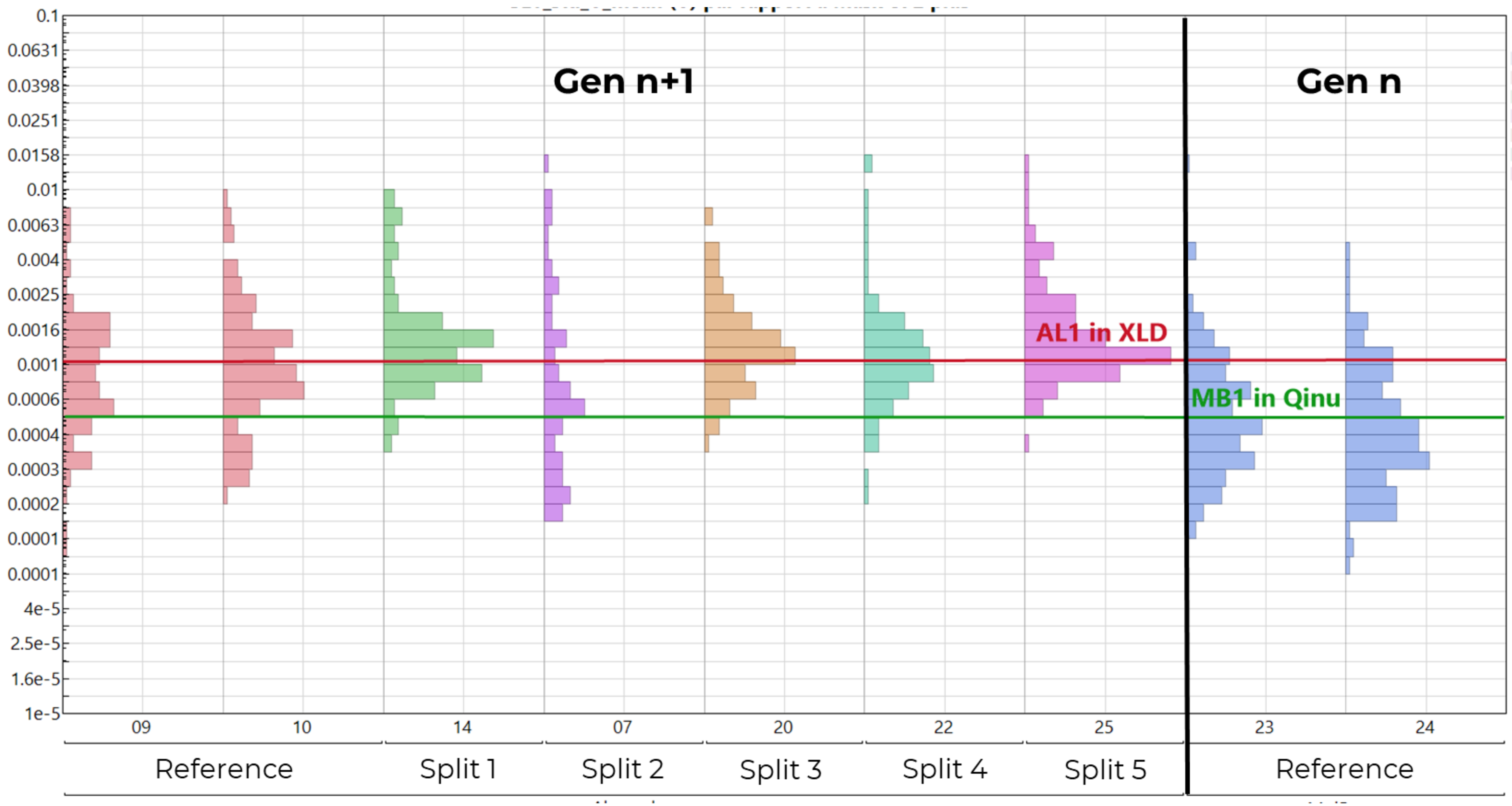

COMMERCIAL FABS

Industrialize

- Quality
- Clock speed
- Scalability
- Cost

High-throughput characterization in the few electron regime

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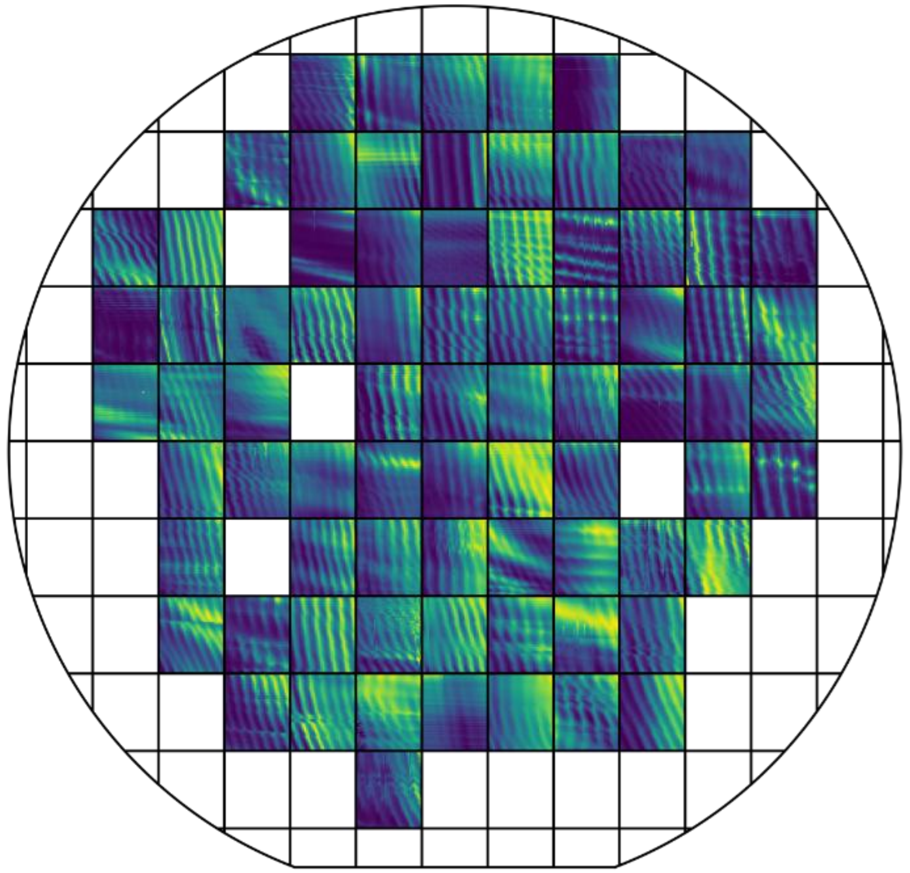
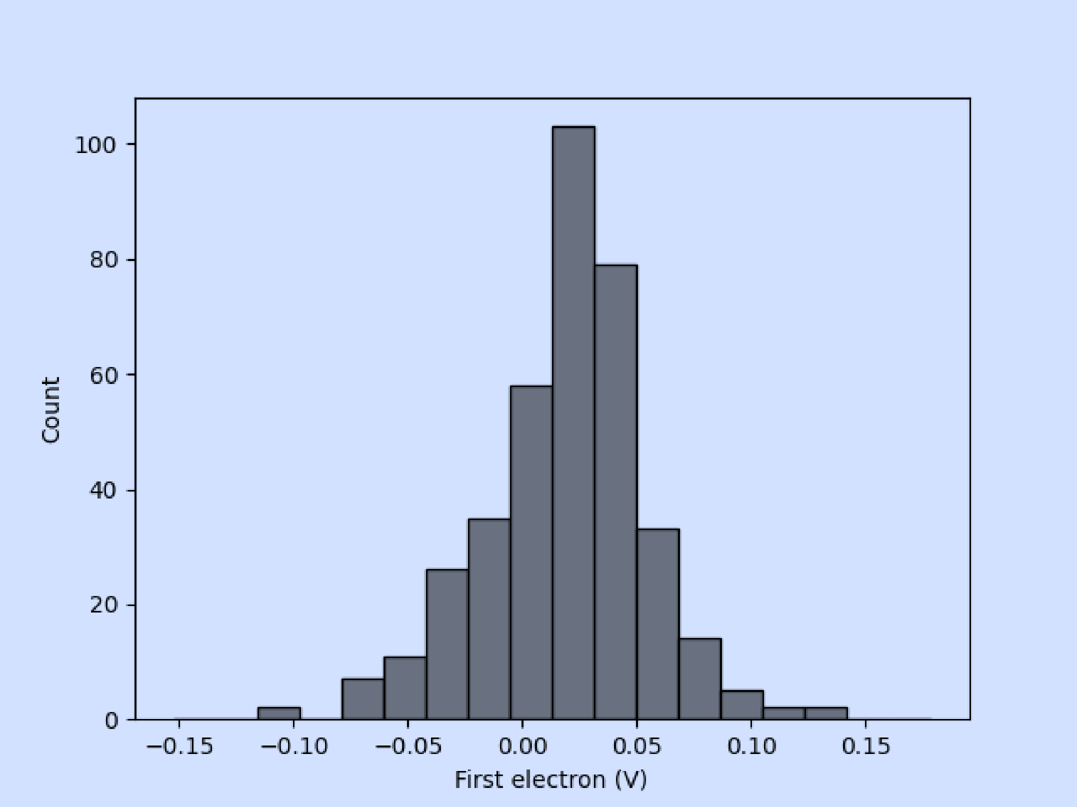
Yield for charge detection of few-electron regime = 69% (377/546 stability diagrams)



First electron position = 0.021V

σ = 26mV

Very low Variability compatible with Qread



Inspired by microelectronics: ITRQS to drive maturity increase and build manufacturable silicon qubits

	2025	2026	2027	2028	2029-30	2031-32
Topology (connection)	2	2	4	4	4	>4
QPU max qubit count	2	128	1k	10k	100k	1M
Pitch FEOL	80nm	80nm	80nm	confidential	confidential	confidential
Pitch MEOL/BEOL	80nm (CA)	80nm (CA, M1)	80nm (M1, M2, CA, V1)	confidential	confidential	confidential
1QBG Fidelity	99%	99,9%	99.99%	99.99%	99.999%	99.999%
2QBG Fidelity	98%	99%	99.9%	99.99%	99.99%	99.99%
Power Dissipated /Qubit	N.A.	0,1mW/qu	0,01mW/qu	confidential	confidential	confidential
Cryostat power @ 500mK	1mW	40mW	100mW	confidential	confidential	confidential
Quantum op. speed (1QBG)	5µs	1µs	500ns	confidential	confidential	confidential
Shuttling	N.A.	1µs / 99%	200ns / 99.9%	50ns / 99.99%	10ns / 99.999%	5ns / 99.999%
Test/Charac (Cryoprober)	2wf/wk charge	3wf/wk charge	2wf/wk spin	confidential	confidential	confidential
3 Sigma(1st e- entry voltage)	200mV	50mV	25mV	10mV	10mV	10mV
Quantum Operations per s	125 kop/s	128 Mop/s	1 Gop/s	confidential	confidential	confidential
Bit extraction rate	100 kbit/s	128 Mbit/s	200 Mbit/s	confidential	confidential	confidential

To build manufacturable qubits

Making quantum large-scale requires large-scale partnerships

1. Fabrication
2. Characterization
3. SDK for software co-development

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THANK YOU FOR YOUR ATTENTION!

The EU-Japan Digital Week is an initiative under the EU-Japan Digital Partnership and is supported by the following projects and organisations

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TAKING EUROPEAN INNOVATION GLOBAL

INPACE
Indo-Pacific-European Hub for Digital Partnerships

JASMINE
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東京大学
THE UNIVERSITY OF TOKYO

SiNANO Institute