
2nd
EU-JAPAN DIGITAL WEEK 2026
23 March - 30 March 2026
Tokyo, Japan
The EU-Japan Digital Week is organised as part of the EU-Japan Digital Partnership

The Future of Compute: From Atomic-Scale Scaling to System-Level Integration

Nadine Collaert, imec

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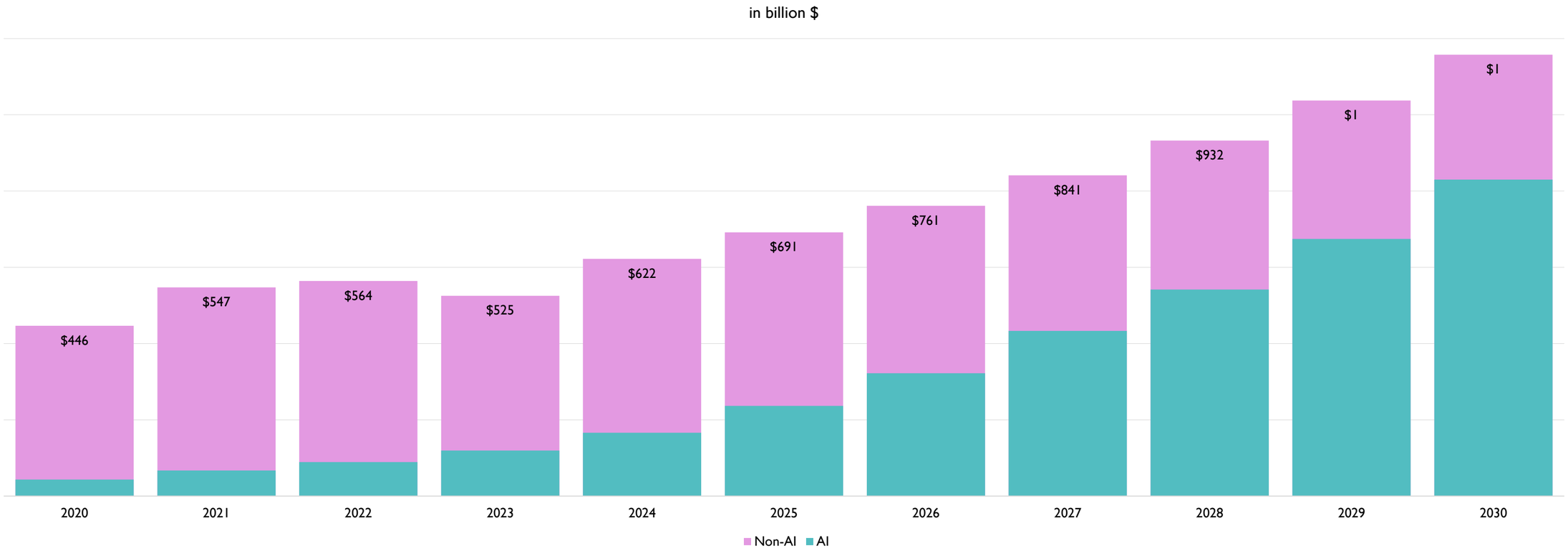
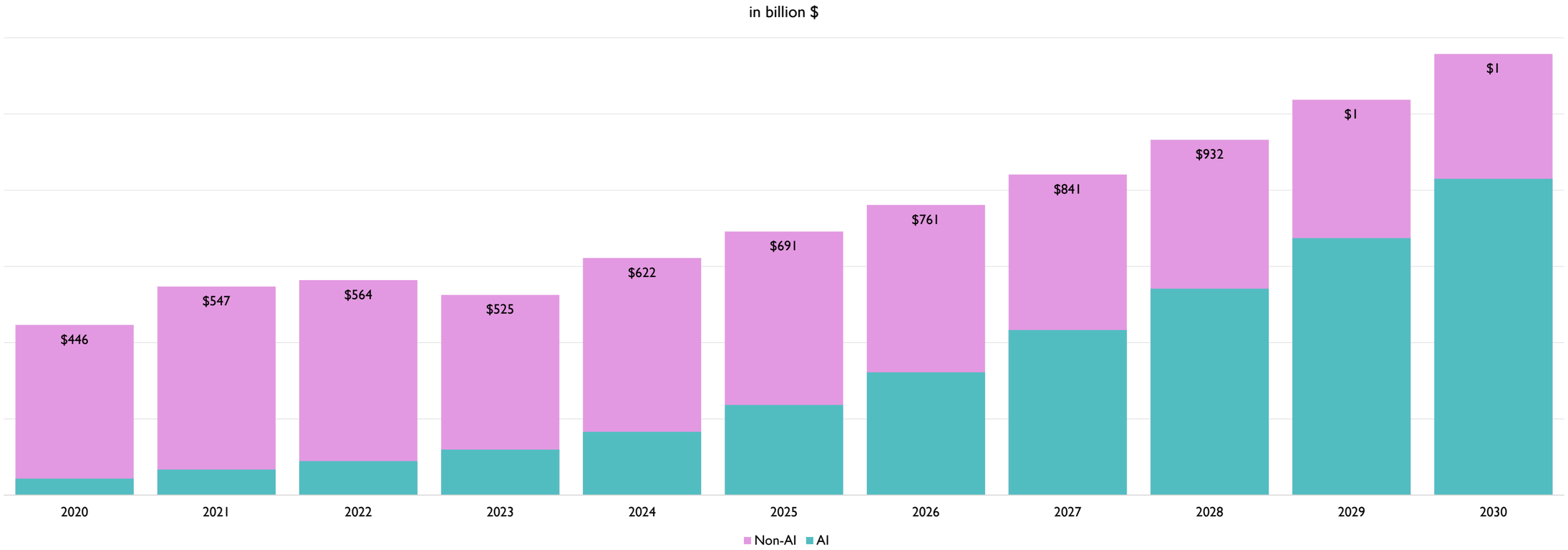
The AI market is expected to drive the semiconductor ecosystem



driving

The AI market is ~~expected to drive~~ the semiconductor ecosystem



Diversified applications drive different system solutions

Hyperscale datacenters

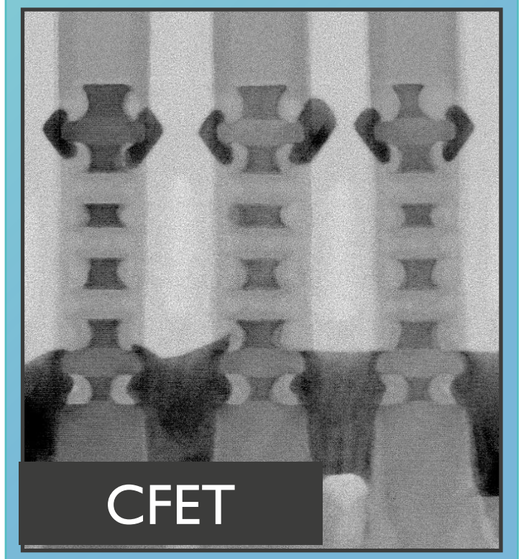
Edge & Cloud datacenters

Autonomous and mobile applications

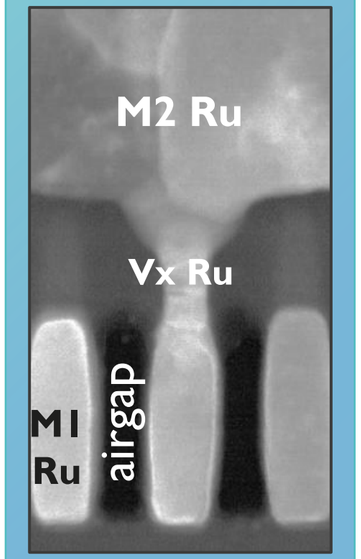
Performance ⟷ **Latency & power**

Technology solutions becoming more sophisticated to support dimensional scaling

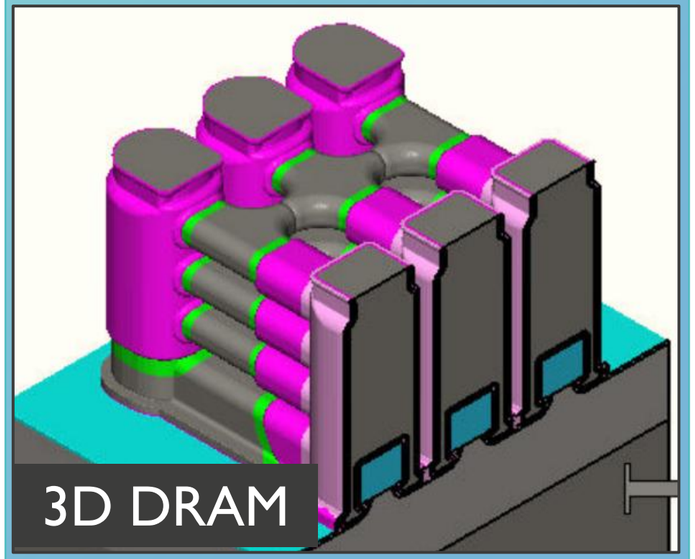
New device architectures



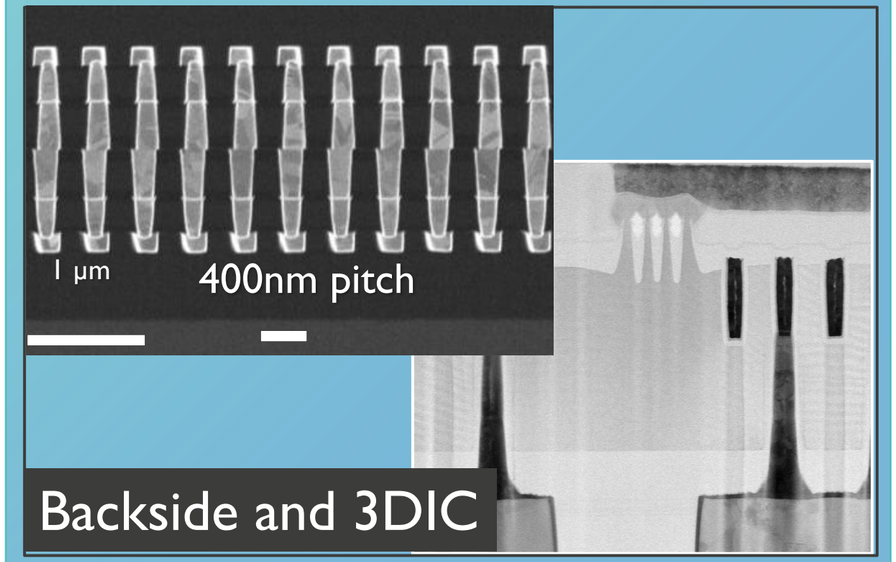
RC boosted interconnect



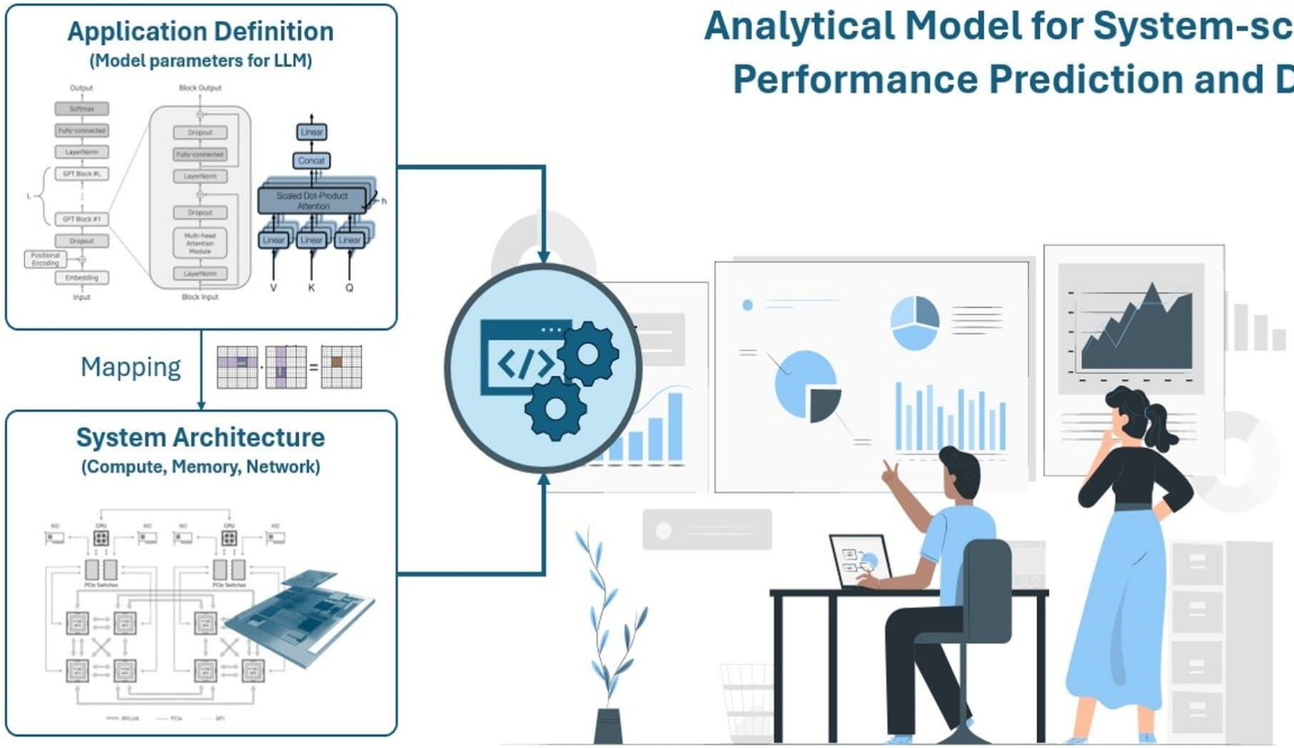
3D-integrated DRAM



Novel Global interconnect solutions



Hardware-software co-design is a must

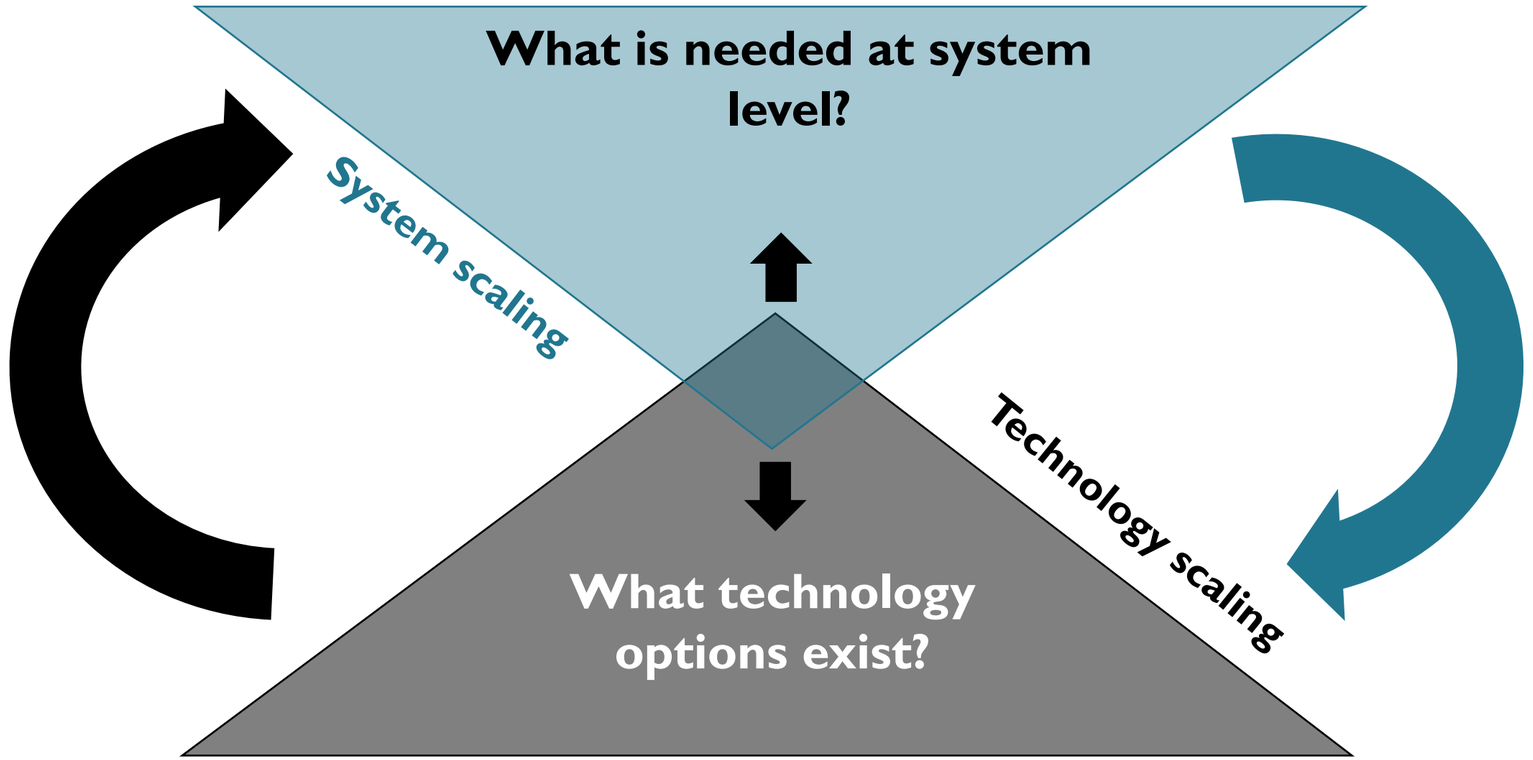


https://www.imec-int.com/en/expertise/compute-system-architecture/imeckelis

Solution needs to come from system-level scaling

System optimization based on off-the-shelve technology

Technology components at Device level impact System performance

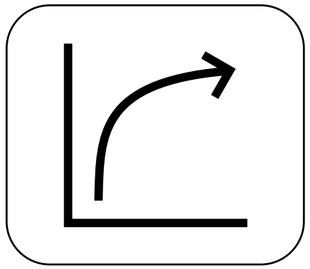
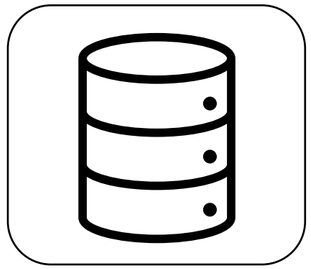
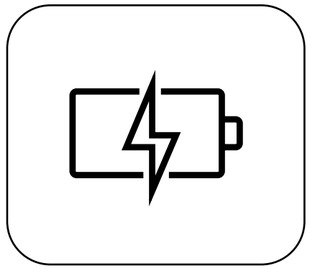
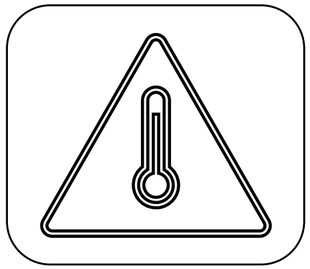
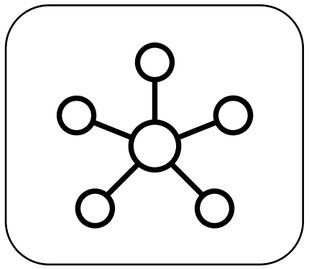
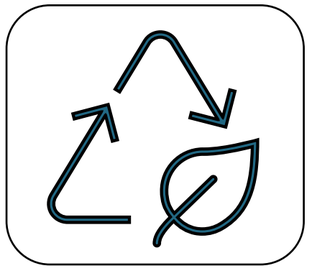


System level architectures and applications drive Technology roadmap

Technology optimization for generic applications

Addressing the system scaling needs

Challenges for future systems

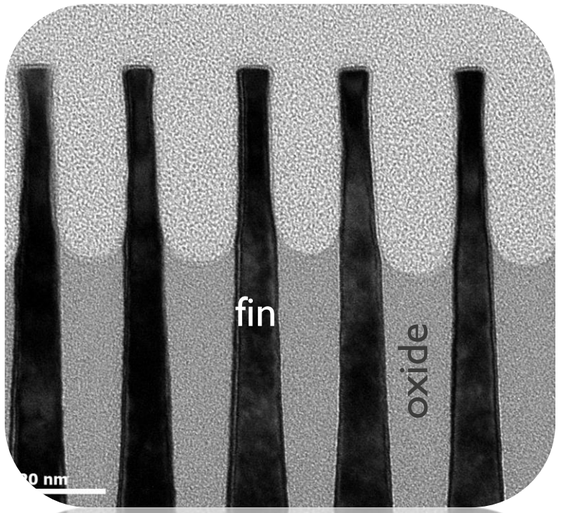
Compute | Memory | Power | Thermal | Connectivity | Sustainable Manufacturing

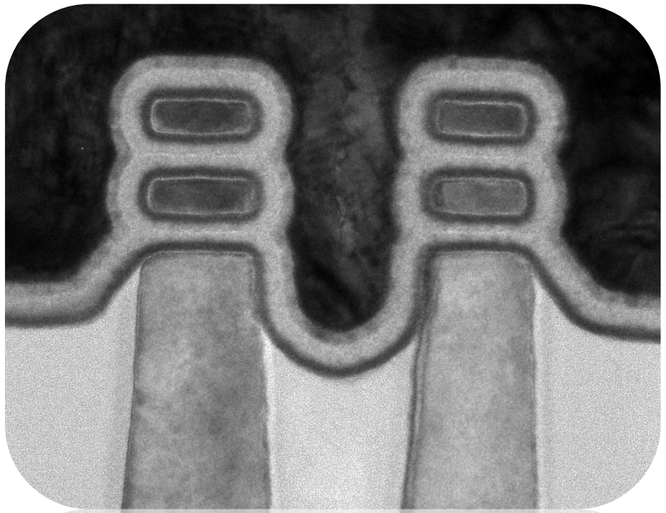
System scaling

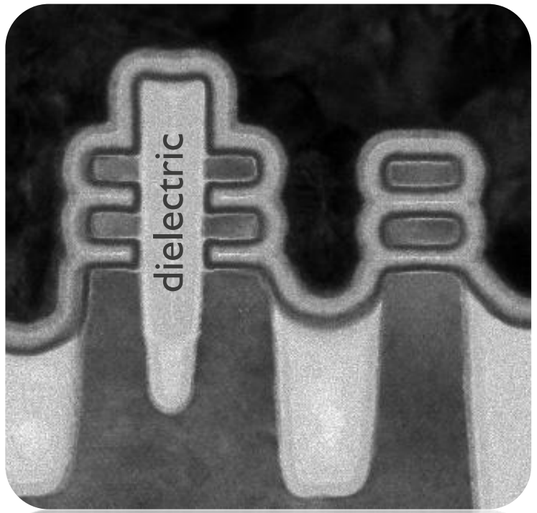
From FinFETs to nanosheets to CFET

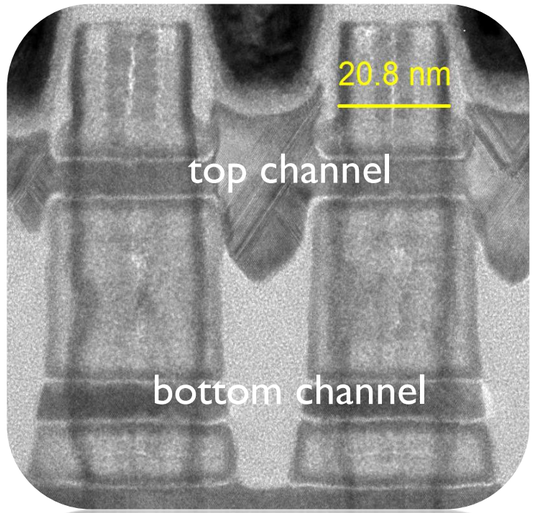
14-3nm | 2nm-10Å | 7-2Å

FinFET | Nanosheets | Forksheets | CFET









N. Collaert, "Advancements in IC Technologies: A look toward the future," in IEEE Solid-State Circuits Magazine, vol. 15, no. 3, pp. 80-86, 2023.

2018	2020	2023	2025	2027	2029	2031	2033	2035	2037	2039
N7	N5	N3	N2	A14	A10	A7	A5	A3	A2	sub-A2

DEVICE AND MATERIAL INNOVATIONS

FinFET → **NanoSheet** → **CFET** → **2DFET, ?, …**

	FinFET			NanoSheet			CFET			2DFET, ?, …	
	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled
											
Metal Tracks	6	6	6	5	5	5	4	<4	<4	<4	<4

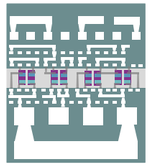
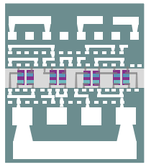
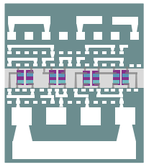
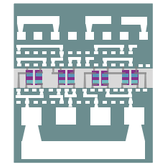
CONTINUED DIMENSIONAL SCALING

0.33NA EUV → 0.55NA EUV → 0.75NA EUV ?

Metal Pitch [nm]	40	28	23	22	21	18	18-16	18-14	16-12	16-12	14-10

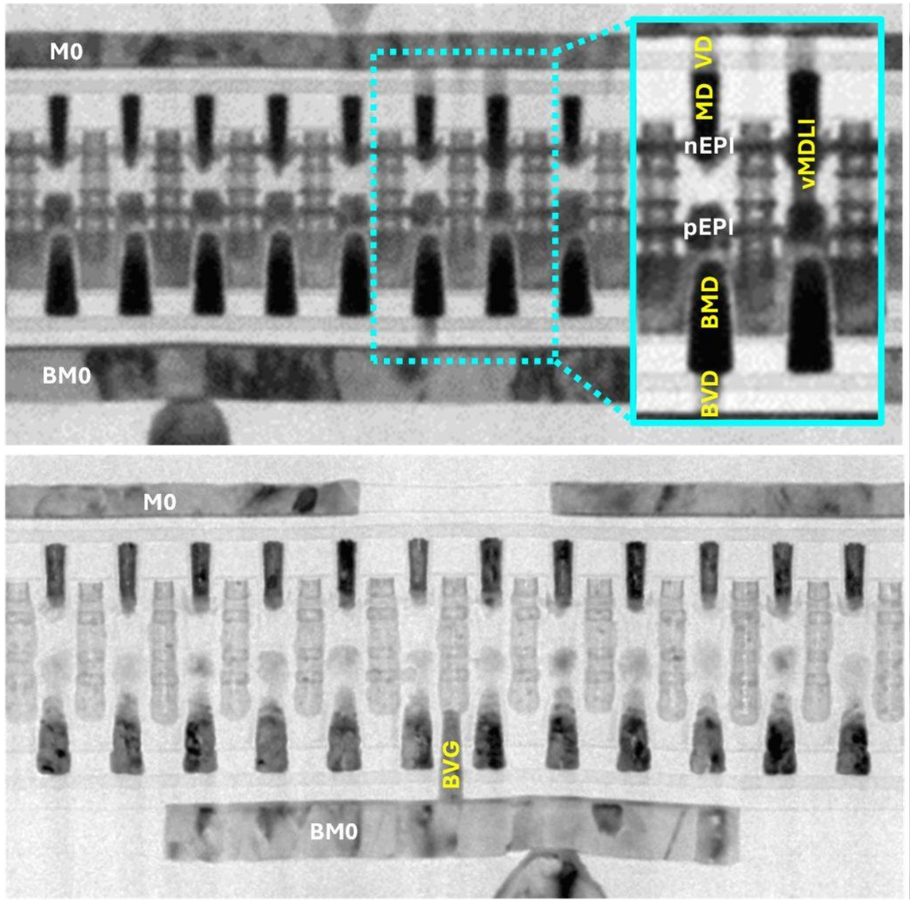
CHIP INTERCONNECT ARCHITECTURE

Back-side Power - Global interconnects → Back-side Power - Local signal lines

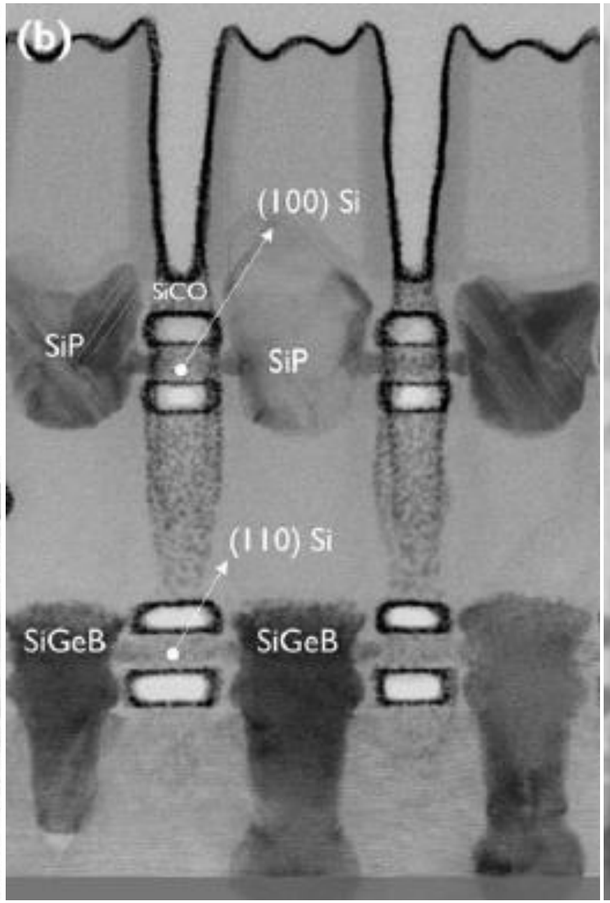
										…
Back-side Metal Pitch estimate [nm]	-	-	160-65	115-45	90-42	40-34	40-28	tbd	tbd		

CFET implementations

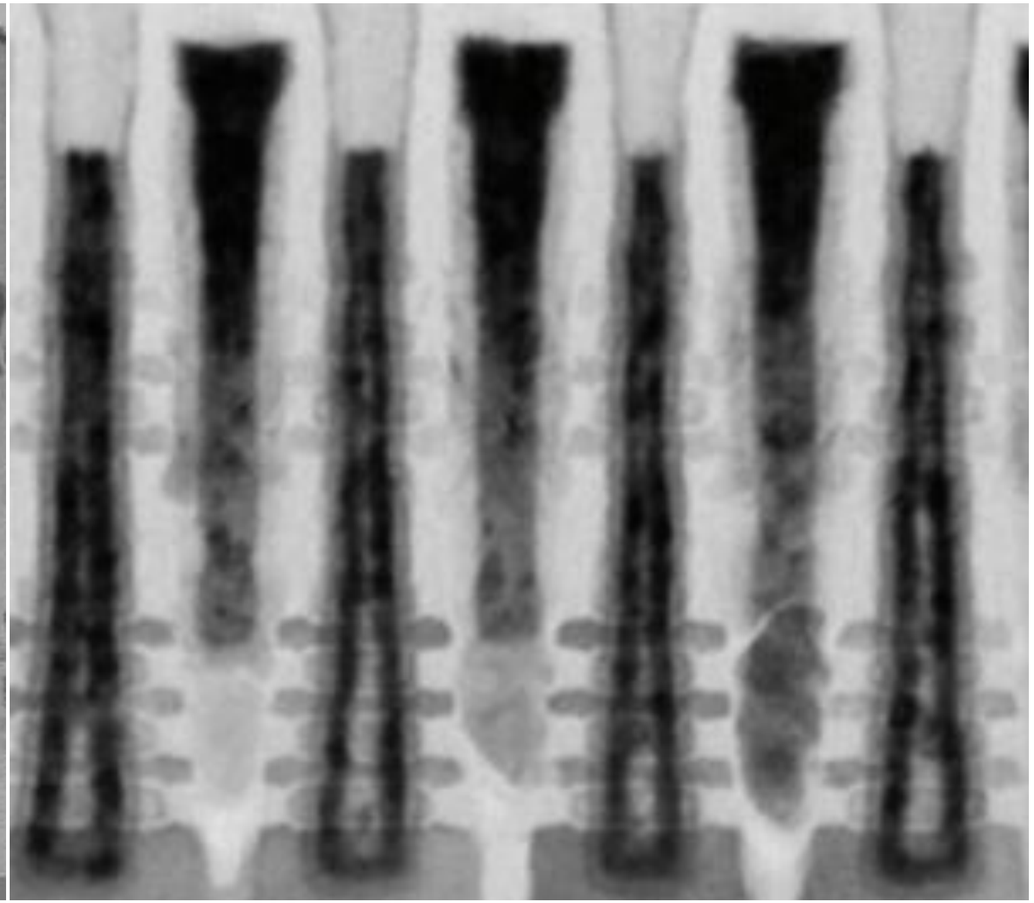
S. Liao et al., IEDM 2024



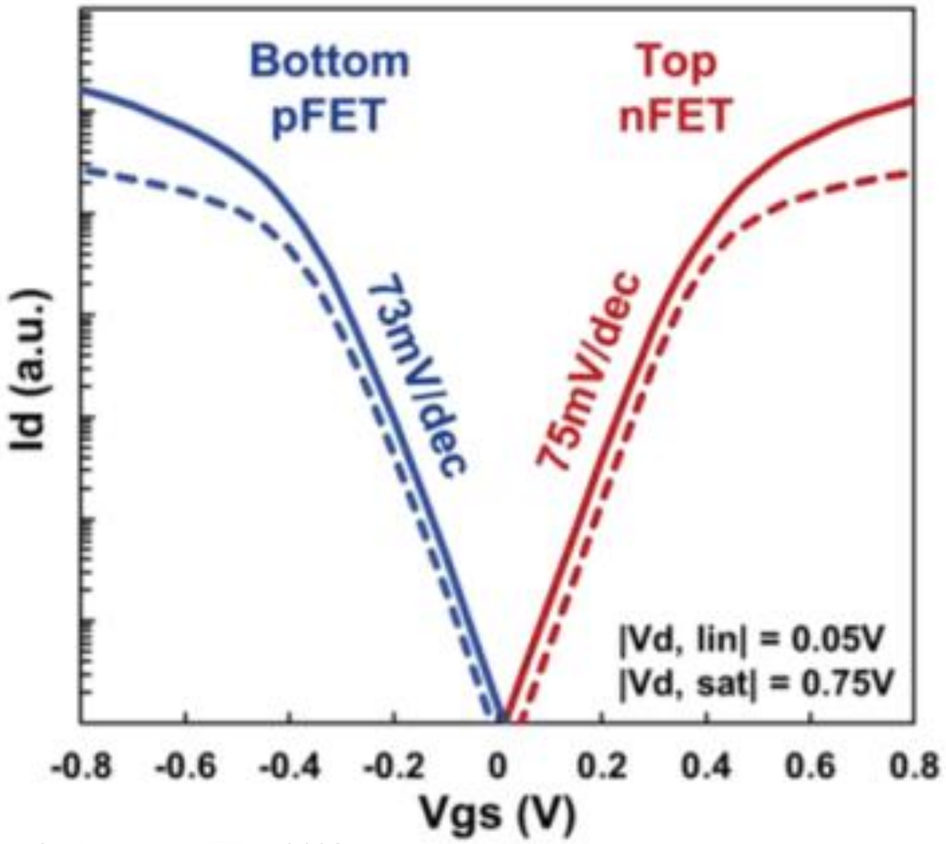
A. Vandooren et al., IEDM 2025



M. Radosavljević et al., IEDM 2023



CFET device performance



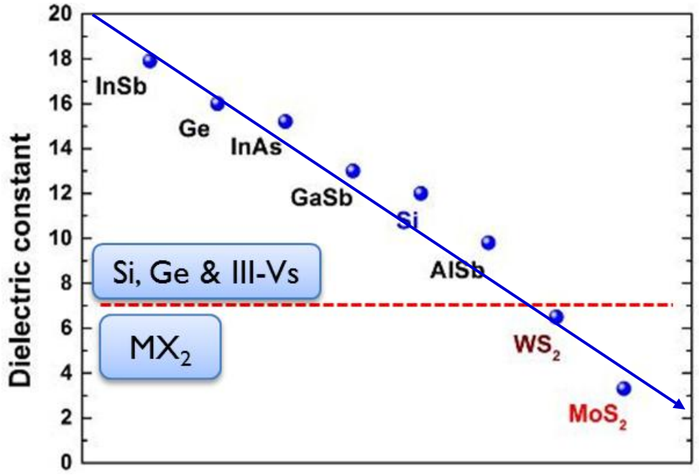
S. Liao et al., IEDM 2023

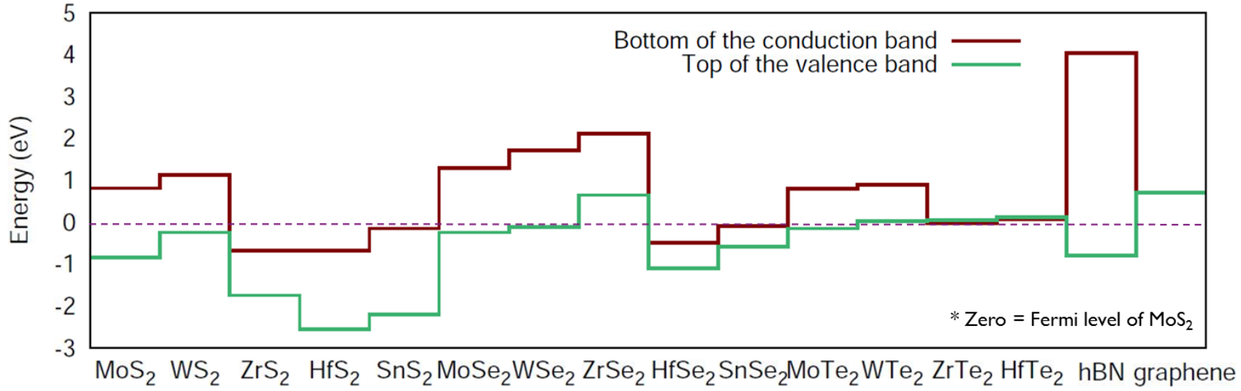
	[1]	[2]
CPP [nm]	48	48
L_G [nm]	15	27
#NS n/p	1/1	1/1
SS_n [mV/dec]	75*	70**
SS_p [mV/dec]	73*	73**
$I_{on,n}$ [mA/μm]	> 1*	0.4**
$I_{on,p}$ [mA/μm]	> 1*	0.1**

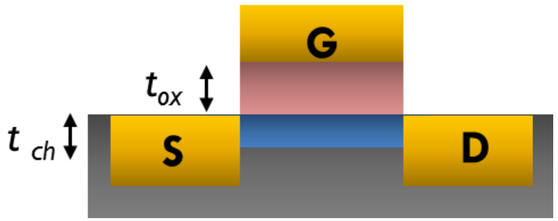
*V_{DS}=±0.75V; **V_{DS}=±0.7V; I_{on} at I_{off}=1nA/μm

[1] S. Liao et al., IEDM 2023; [2] H. Mertens et al., VLSI Symp. 2023

2D materials to extend the roadmap







Characteristic length of short channel FETs:

$$\lambda = \sqrt{\frac{\epsilon_{ch}}{\epsilon_{ox}} t_{ch}.tox}$$

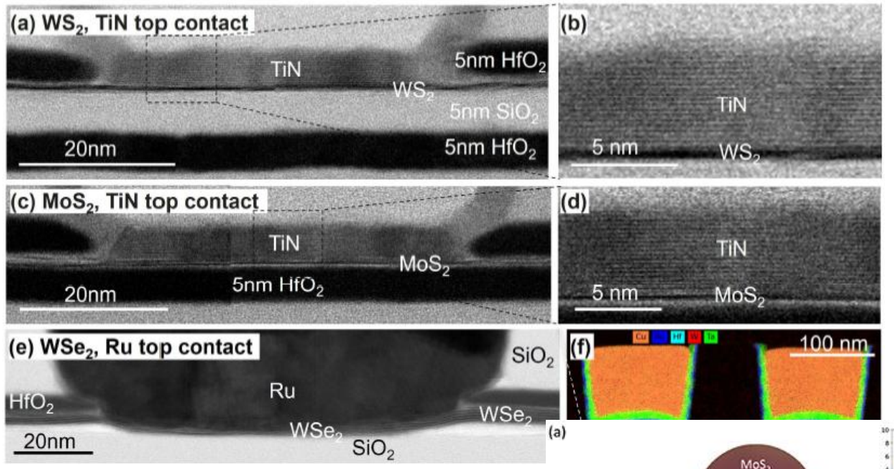
Expect reduced short channel effects in planar devices

because they are ultra-thin materials

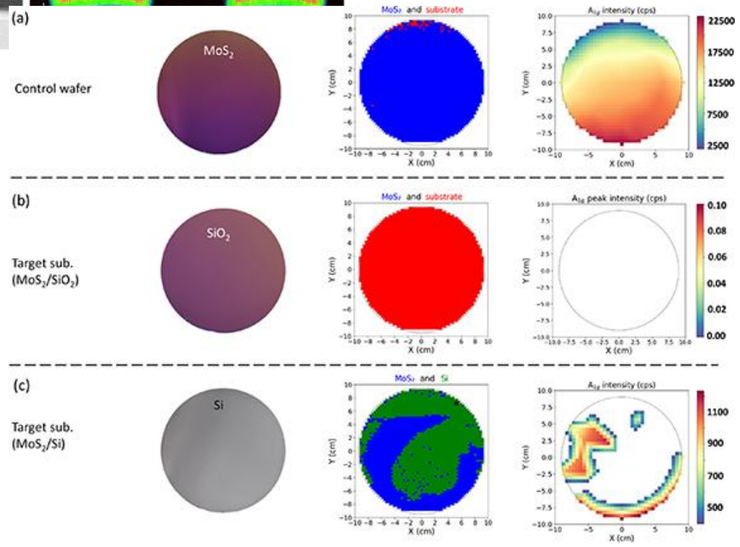
Choice of bandgaps and band alignment

No/few dangling bonds at interfaces

Progress in 2D materials

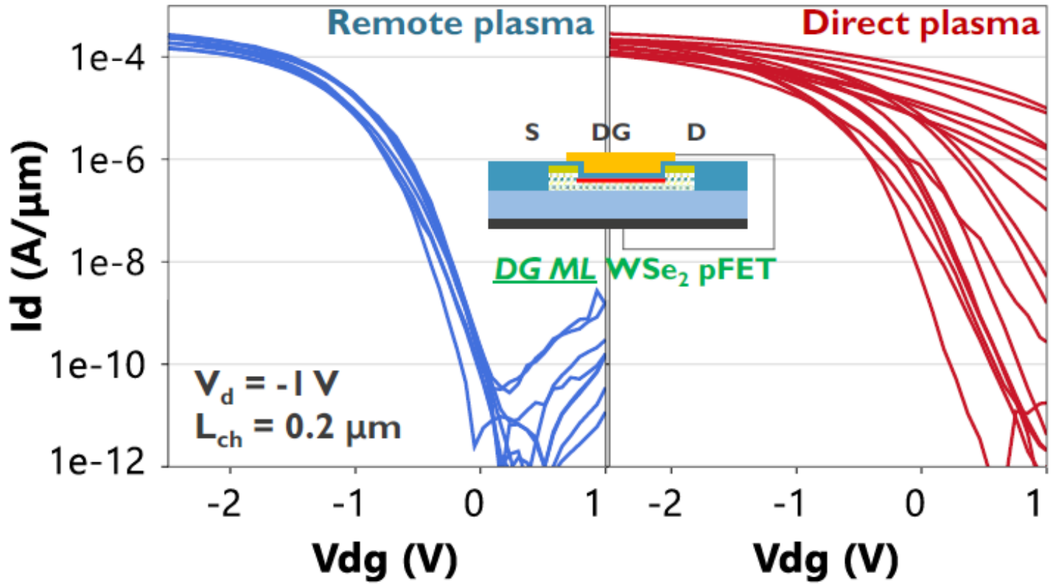


Q. Smets et al., IEDM 2025.



Paul Brunet *et al* 2025
2D Mater. **12** 035013

T.D. Ngo et al., IEDM 2025.



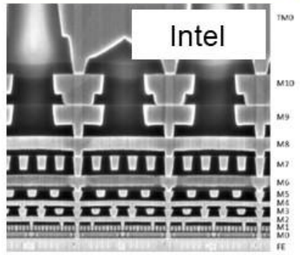
- Progress in key device modules: gate stack, contacts, layer transfer
- Progress in enabling high-performant pFET

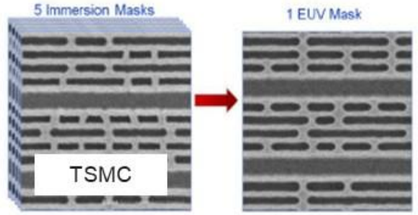
Industry BEOL trends

Courtesy: Z. Tokei (imec)

~36-40nm BEOL pitch

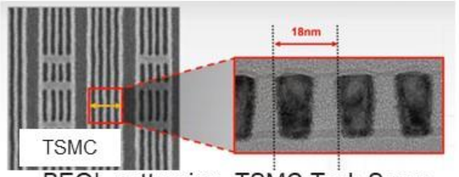
10nm technology, C. Auth et al. IEDM 2017





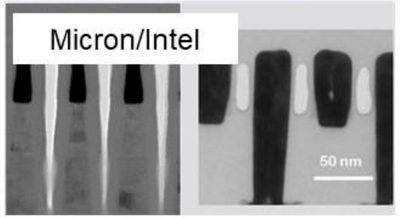
5nm CMOS, G. Yeap et al. IEDM2019

<20nm pitch

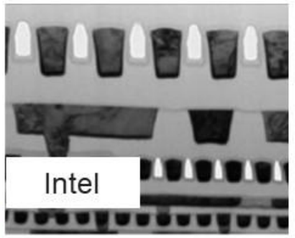


BEOL patterning, TSMC Tech Symp. 2020

AGs in memory & logic

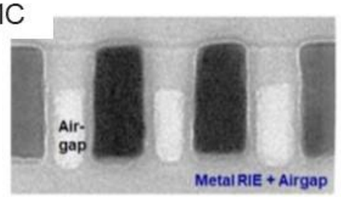


25nm NAND using air gaps K. Prall/K. Parat IEDM2010



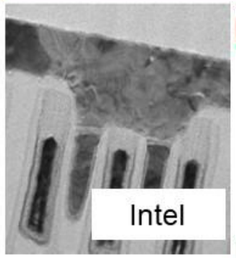
K. Fisher et al., 14nm, IITC2015

TSMC

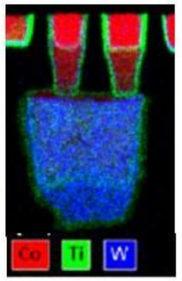


Y.J. Mii et al. Keynote, VLS022

Co interconnects



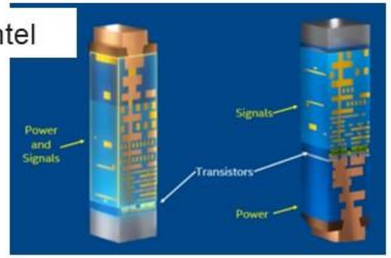
Self- aligned contact, C. Auth et al. IEDM 2017



Reliability of Co, F. Griggo et al. IRPS 2018

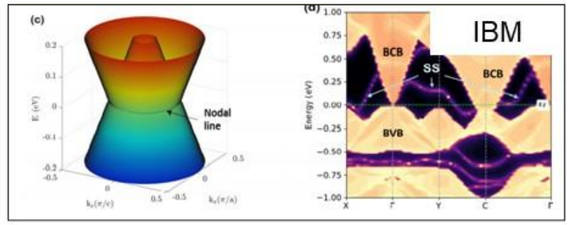
Backside Power Delivery

Intel

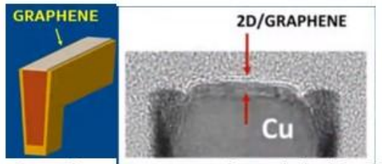


M.C. Mayberry, Keynote IITC 2020

New materials on the horizon

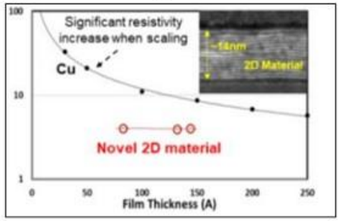


Topological semi-metal, C.T. Chen et al. IEDM2020



Intel

Graphene capped metal, R. Chau et al. Keynote IEDM2019



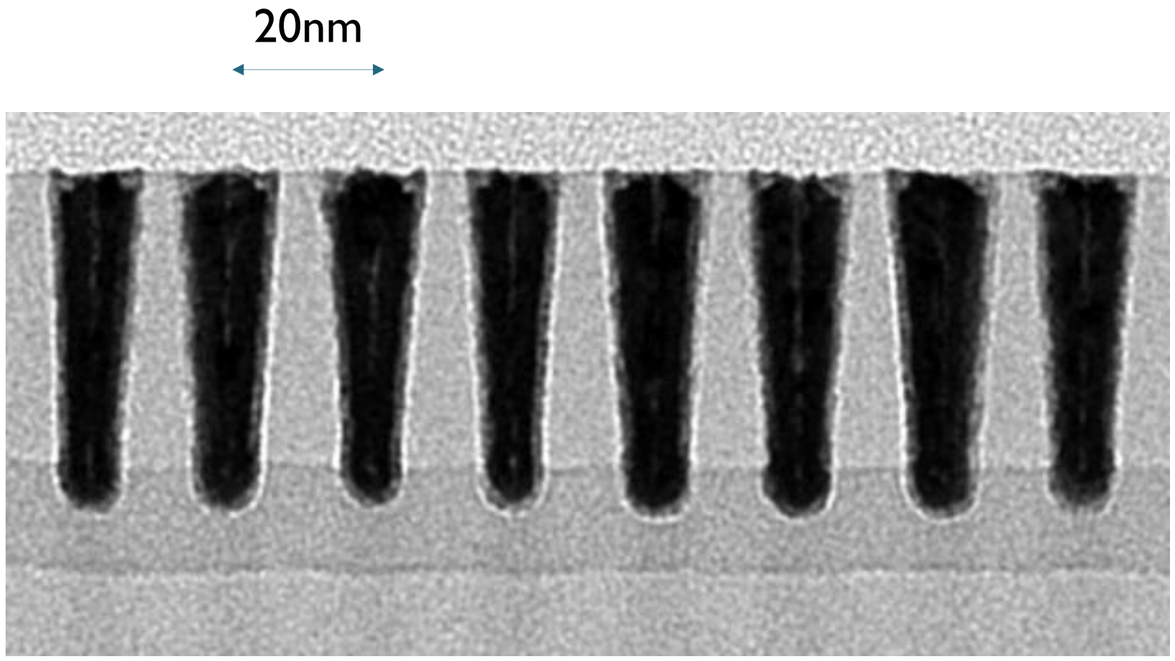
TSMC

New conductor, Y.J Mii Keynote VLSI2022

Pitch scaling, airgaps both in memory and logic, new materials

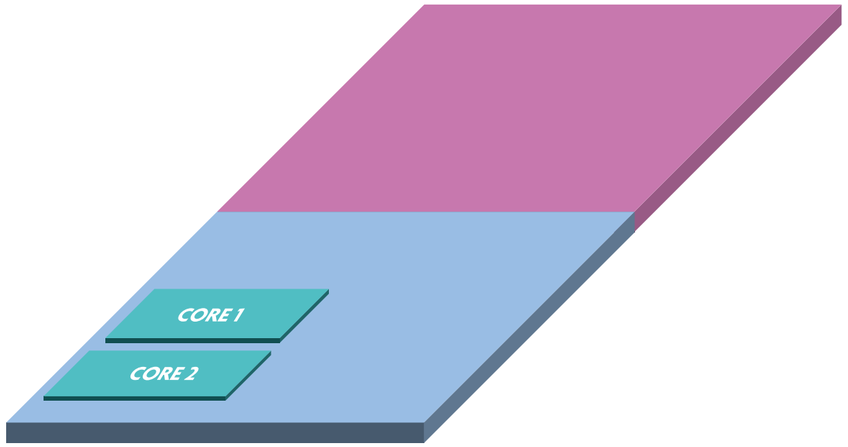
Lithography is still key enabler

Courtesy of ASML

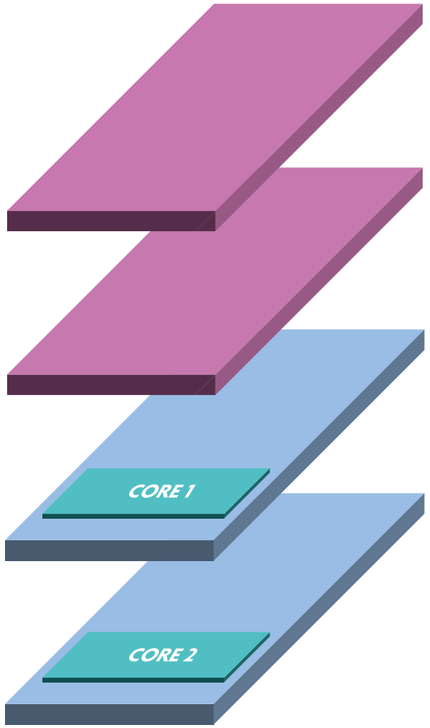


https://www.imec-int.com/en/press/imec-demonstrates-electrical-yield-20nm-pitch-metal-lines-obtained-high-na-euv-single

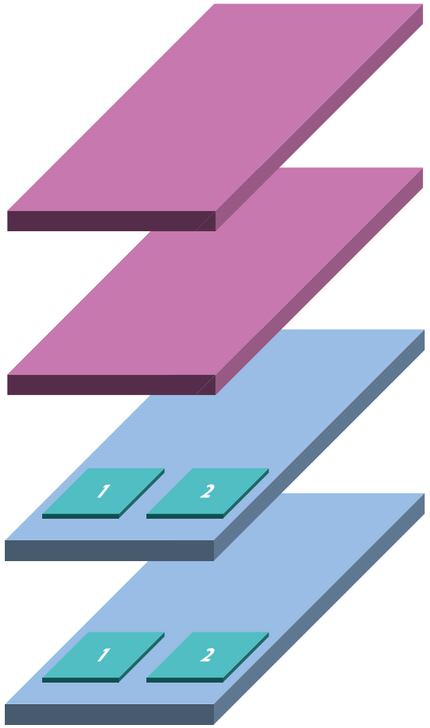
Taking 3D to the next level



2D
(or 2.5D chiplet)

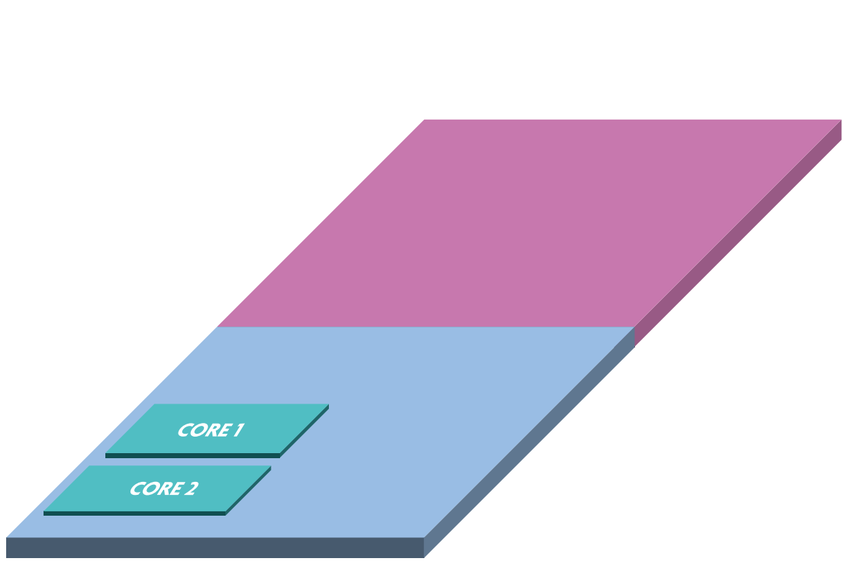


3D stacked
system

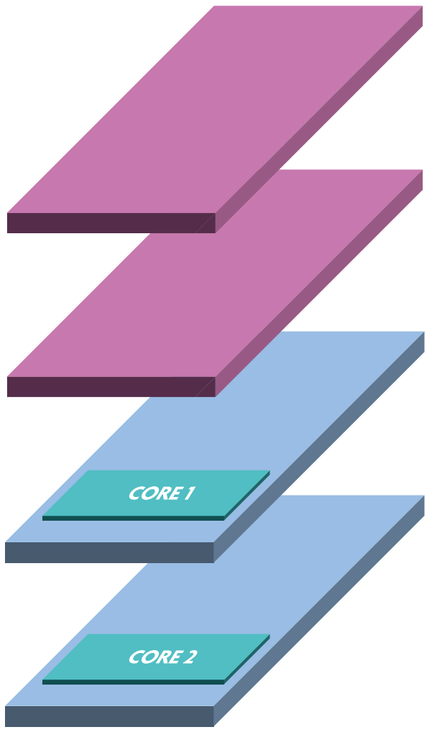


CMOS 2.0 Compute
system

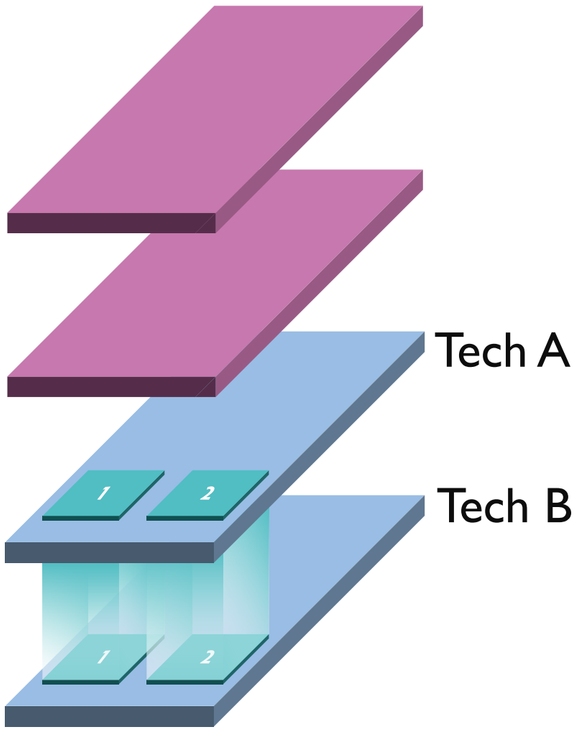
CMOS 2.0 uses functional specialization per tier



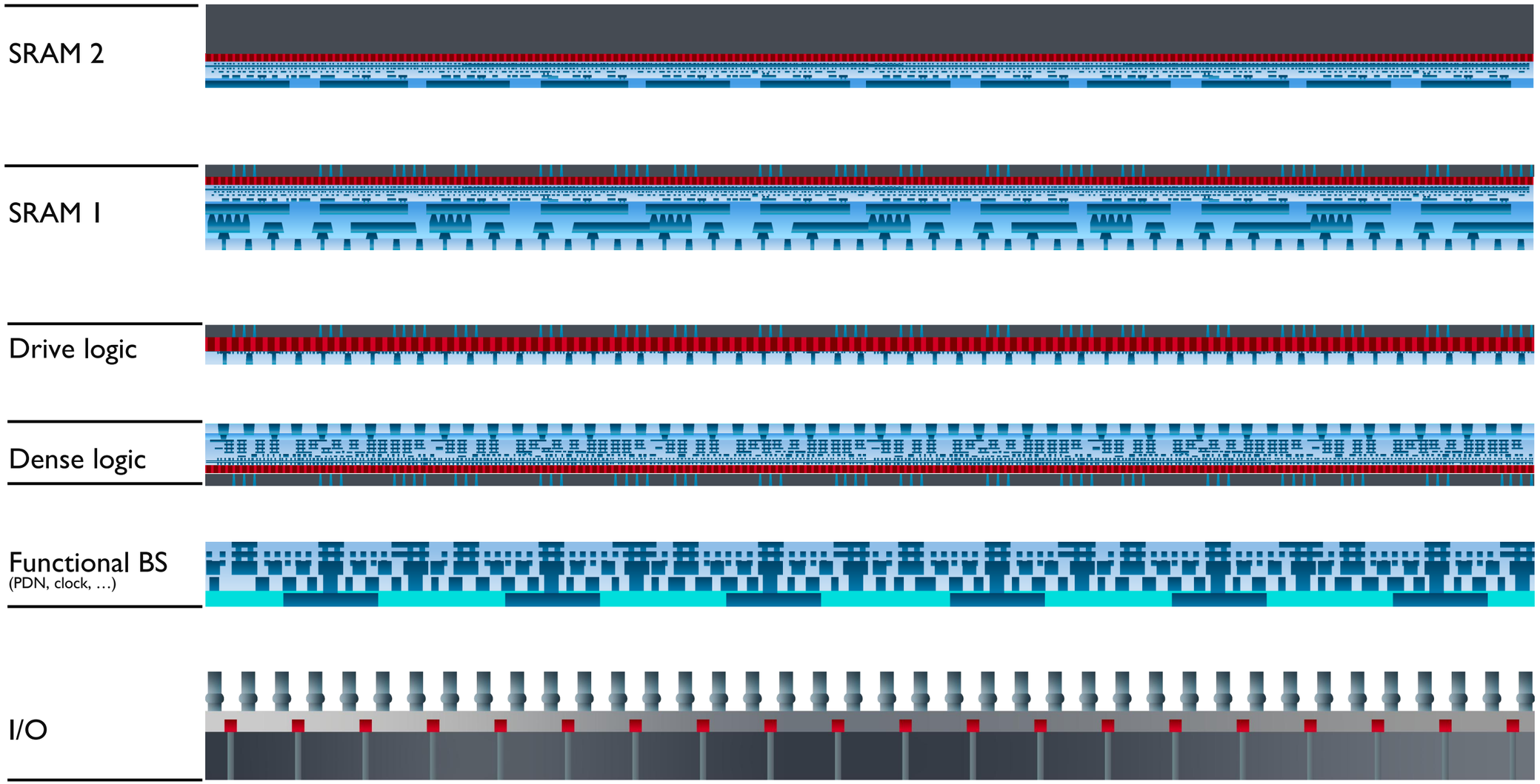
2D
(or 2.5D chiplet)

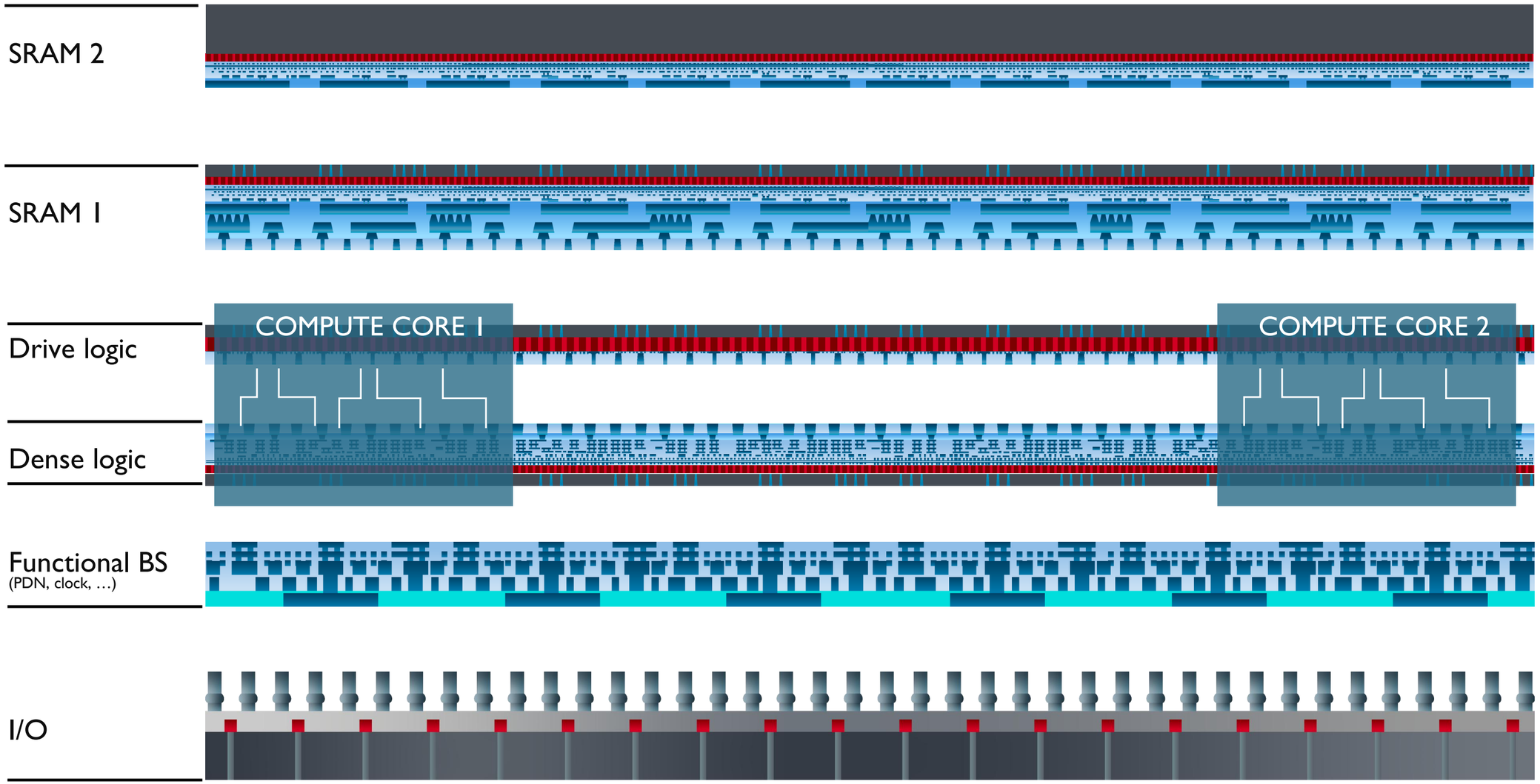


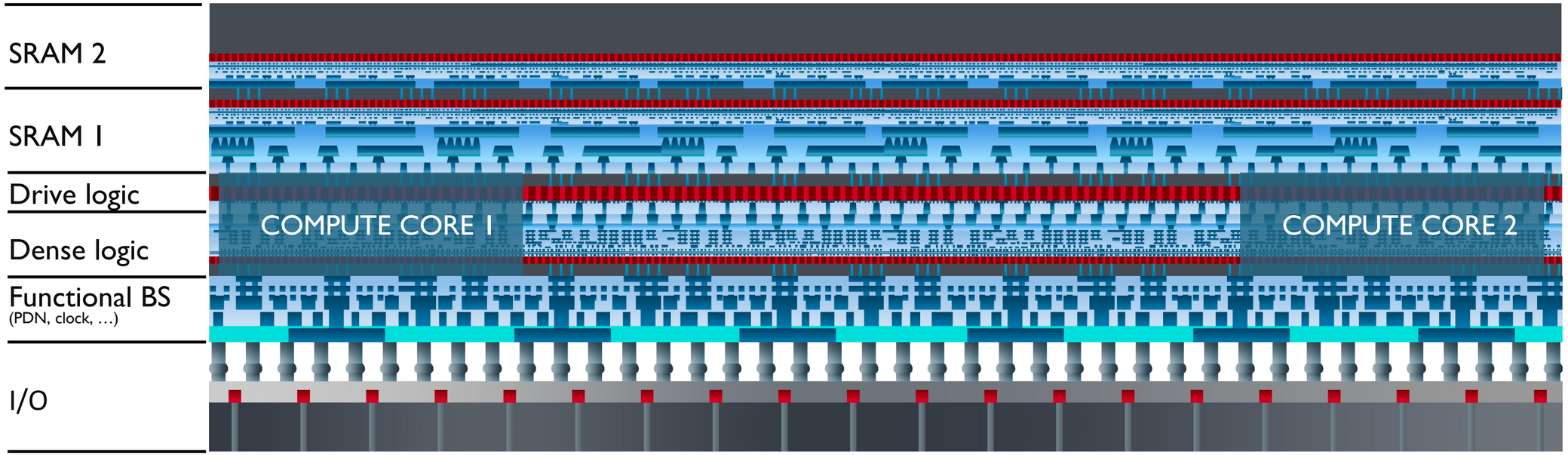
3D stacked
system



CMOS 2.0 Compute
system

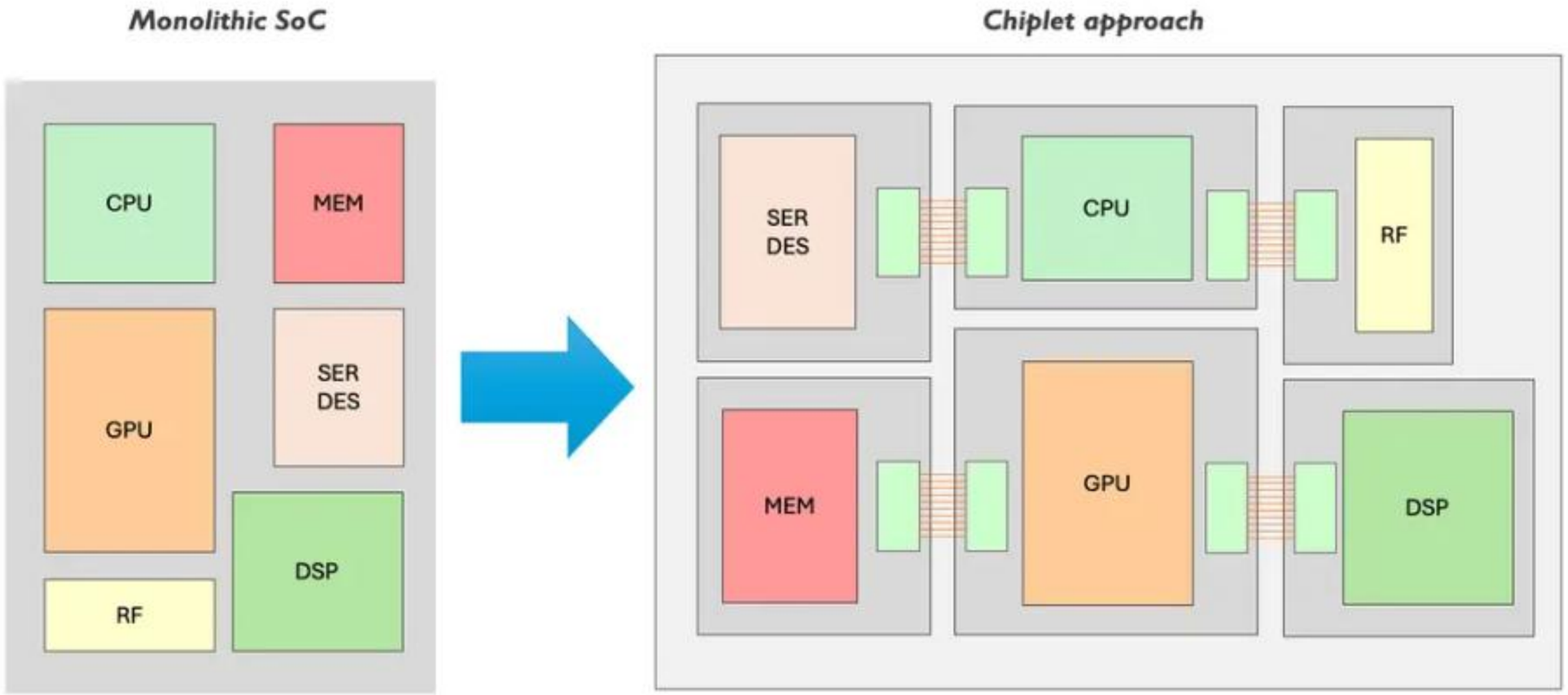

SRAM 2
SRAM 1
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O


SRAM 2
SRAM 1
COMPUTE CORE 1
COMPUTE CORE 2
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O


SRAM 2
SRAM 1
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O
COMPUTE CORE 1
COMPUTE CORE 2

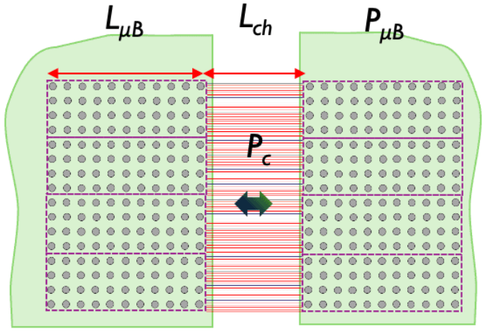
Heterogeneous integration as key enabler

Chiplets offer a modular system

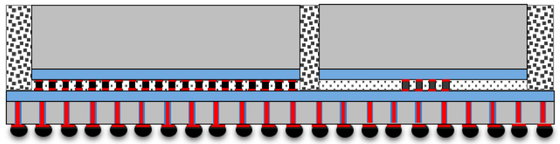


https://www.imec-int.com/en/articles/chiplets-piecing-together-next-generation-chips-part-i

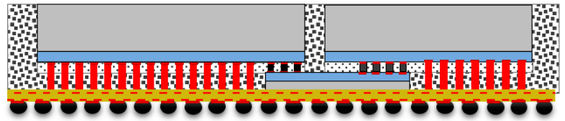
2.5D interposers

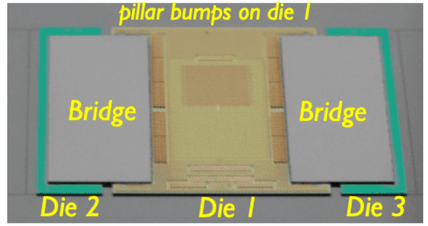


2.5D Si interposer

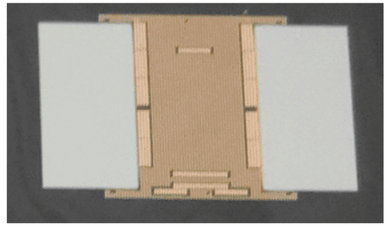


Fan-out WLP with embedded Si-bridge interposer

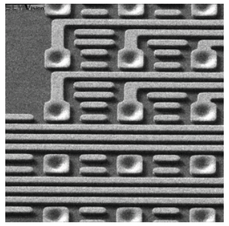




Die placement and bridge bonding

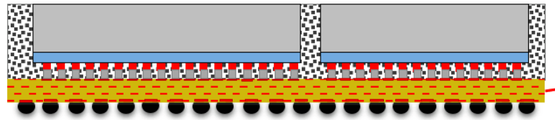


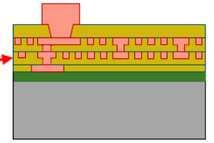
Post molding and back grinding



2 µm Line/Space
Semi-additive RDL

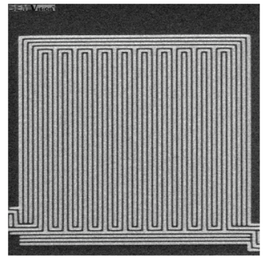
Fine pitch Cu/polymer RDL-first FOWLP



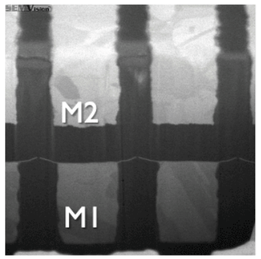


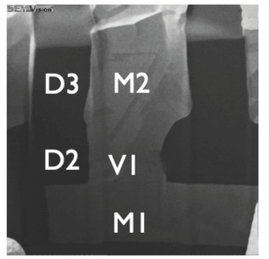
"Damascene"
RDL-first
on carrier wafer

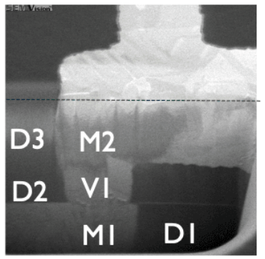
Line/Space scaling: 2 ⇒ 1 µm ⇒ 0.5µm



1µm Line/Space





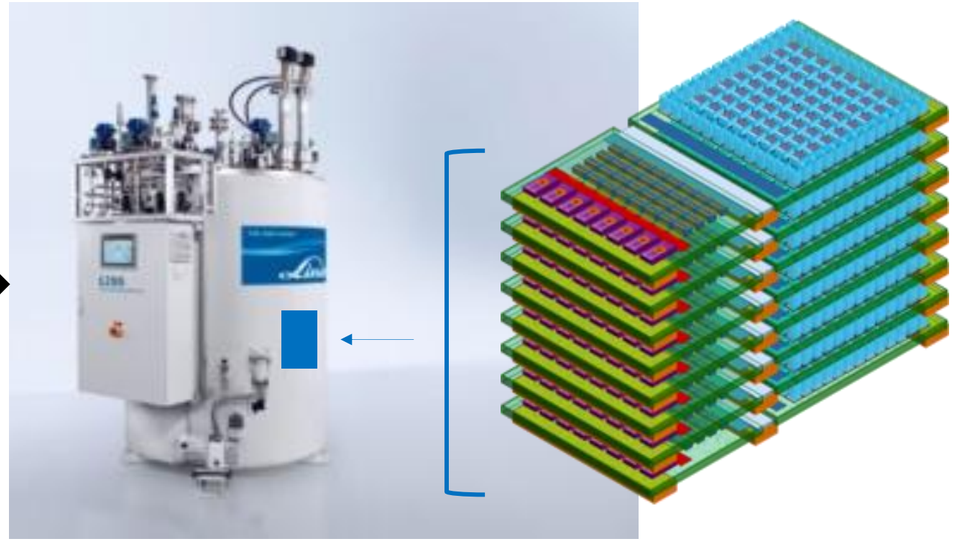


Multilayer Single and Dual Damascene metal integration

Making different machines

Datacenter in a shoebox

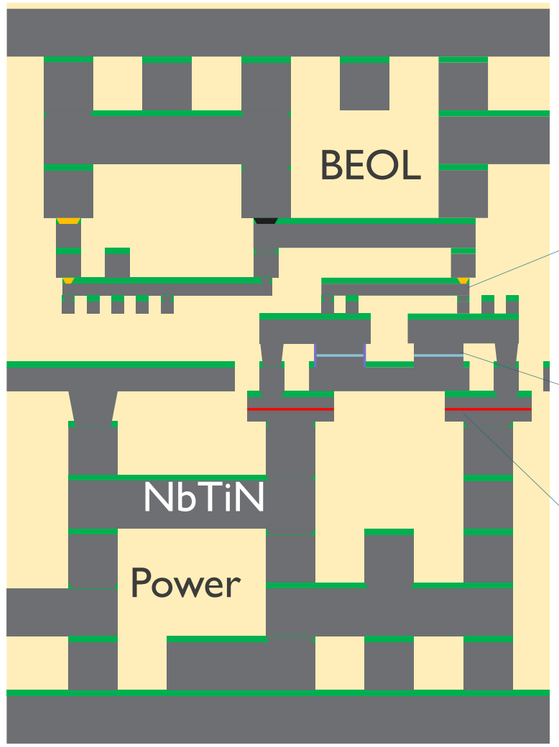
The same performance as NVIDIA EOS: 79.32 ExaFLOPS



18 Trillion devices 150 x 320 x 100 mm

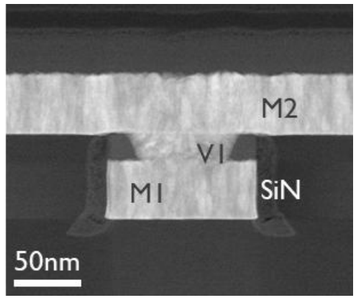
Superconducting digital logic

Production process vision

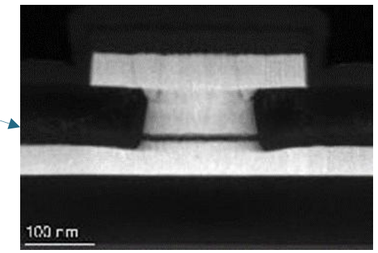


400 MJJ/cm^2 @ 30 GHz

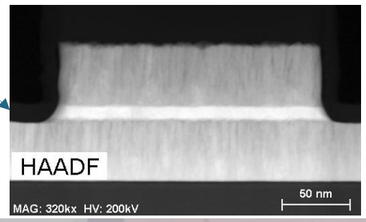
NbTiN wires & vias



NbTiN/aSi JJ



NbTiN/HZO/NbTiN cap



Imec 28 nm 300 mm SCD process

Only one new material, NbTiN

Fully compatible with CMOS process

Computational density the same as 7nm CMOS

Compatible with Place & Route

Take-aways

Conclusions

- AI-driven compute demand is exploding, outpacing Moore's Law and pushing energy consumption to unsustainable levels
- System-level scaling is essential, device innovation alone is no longer sufficient.
- Key challenges include:
  - Compute density
  - Power delivery
  - Thermal management
  - Memory bandwidth
  - Interconnect fabric
- Solutions require cross-technology co-optimization (XTCO) across materials, devices, architecture, and software.

THANK YOU FOR YOUR ATTENTION!

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