
2nd
EU-JAPAN DIGITAL WEEK 2026
23 March - 30 March 2026
Tokyo, Japan
The EU-Japan Digital Week is organised as part of the EU-Japan Digital Partnership

Semiconductor Workshop

“Japan-EU Cooperation on Advanced Computing, Advanced Functionalities and Semiconductor Value Chain”

Semiconductor Technology, value chain and projects for possible international cooperation

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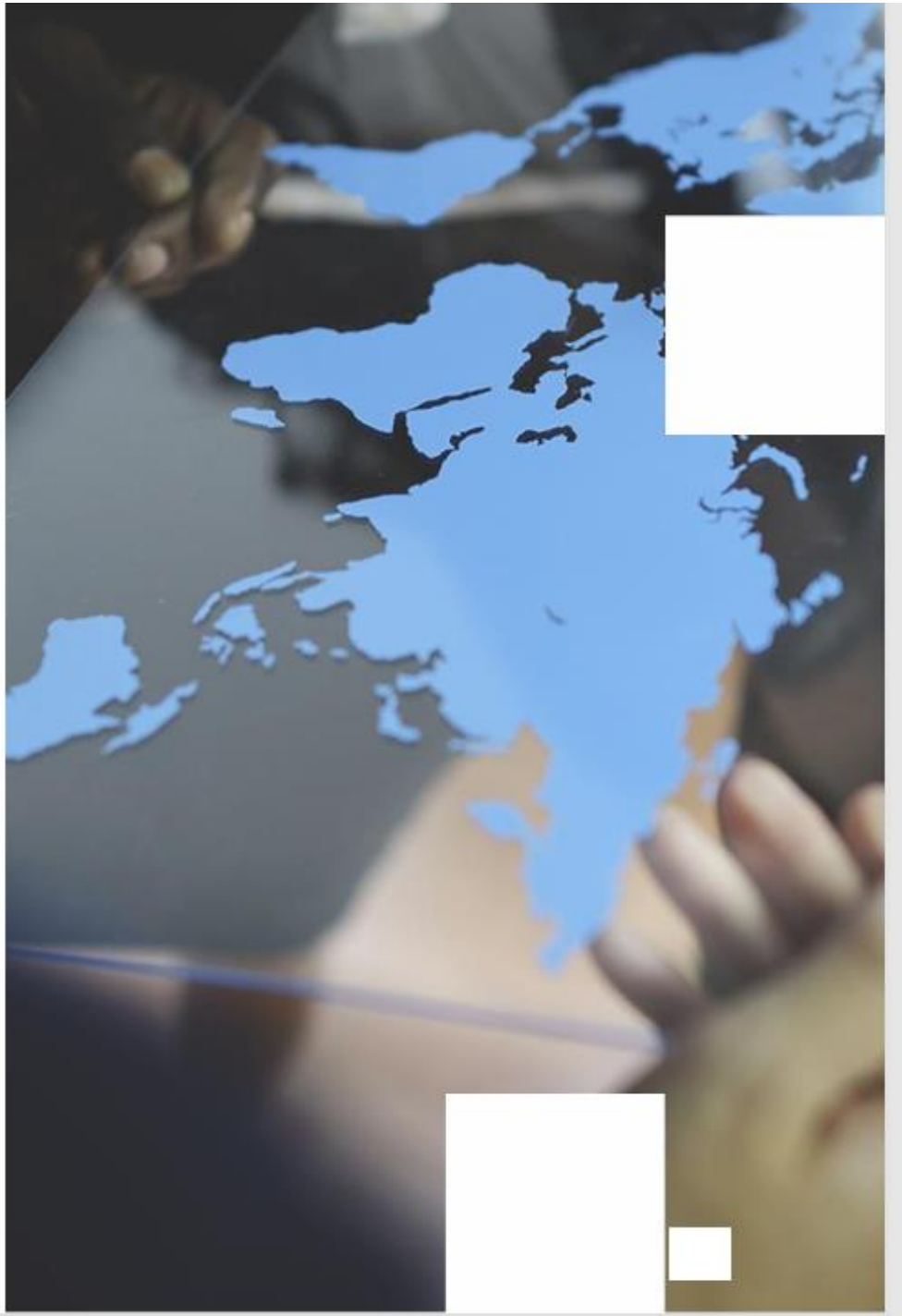
Projects for possible international cooperation

Horizon Europe INPACE & JASMINE projects

INPACE
Indo-Pacific-European Hub for Digital Partnerships: Trusted Digital Technologies for Sustainable Well-Being

- Coordination and Support Action
- Jan 2024 - June 2027 (3,5 years)
- 21 consortium partners
- 13 European and Indo-Pacific countries
- Funding: Horizon Europe and Swiss State Secretariat for Education, Research, and Innovation - SERI



INPACE

INPACE: a forward-looking project

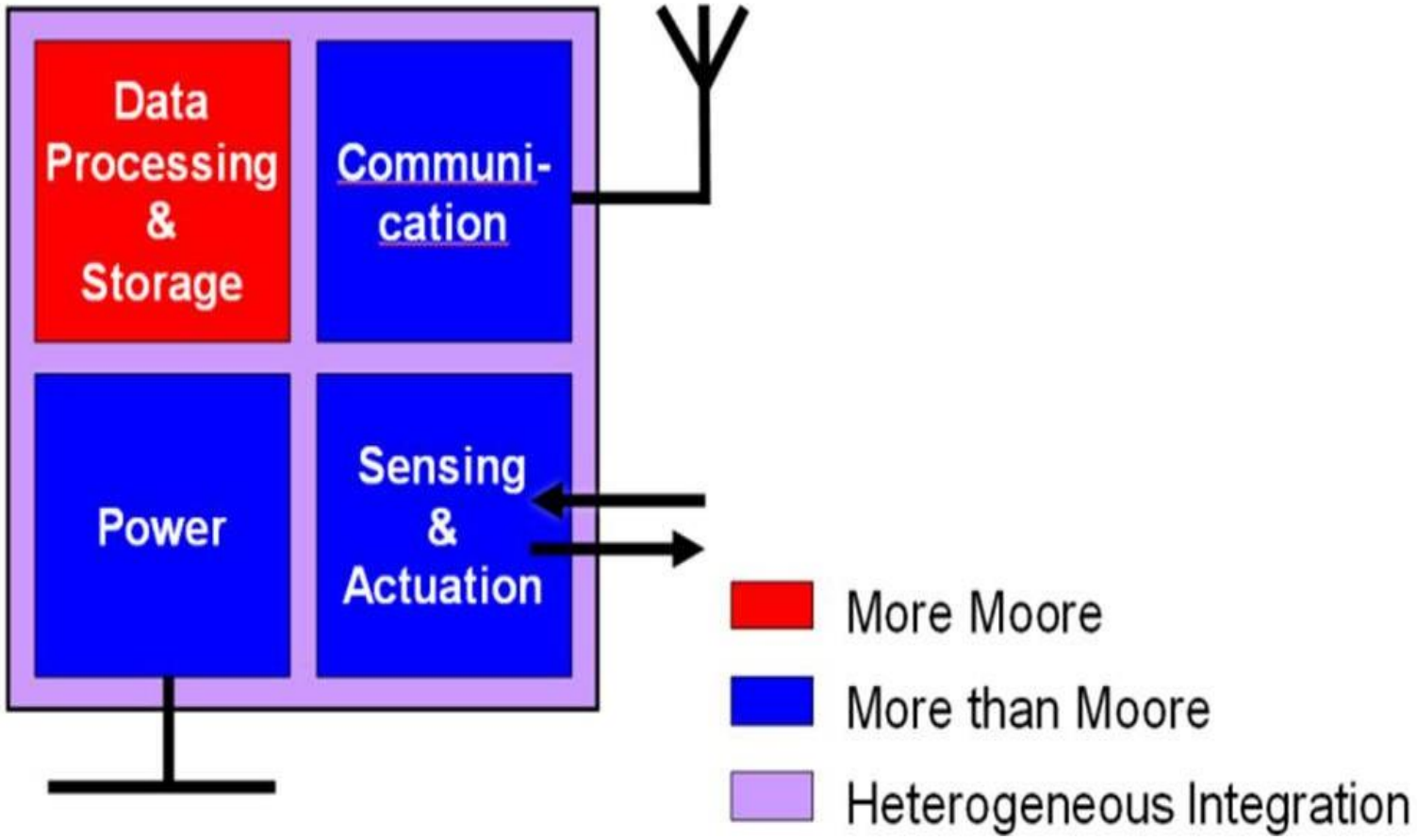
Connecting leading experts through content-related groups, across the Indo-Pacific and Europe, that discuss technology trends, align policy and research, provide insights for policy-makers, and foster collaboration among key players to drive innovation and future joint initiatives.

Building the Indo-Pacific European Hub, engaging with broader communities, for **bottom-up value-added feedback** to the DPs and TTC, and for **continuation after the project**

Directly supporting the individual DPs and TTC through events (workshops, webinars, virtual fairs both with a focus on specific topics of prime interest and across topics and countries), facilitating pilot projects with external collaboration partners.

INPACE Thematic Clusters

INPACE Cluster 4



INPACE Semiconductor thematics

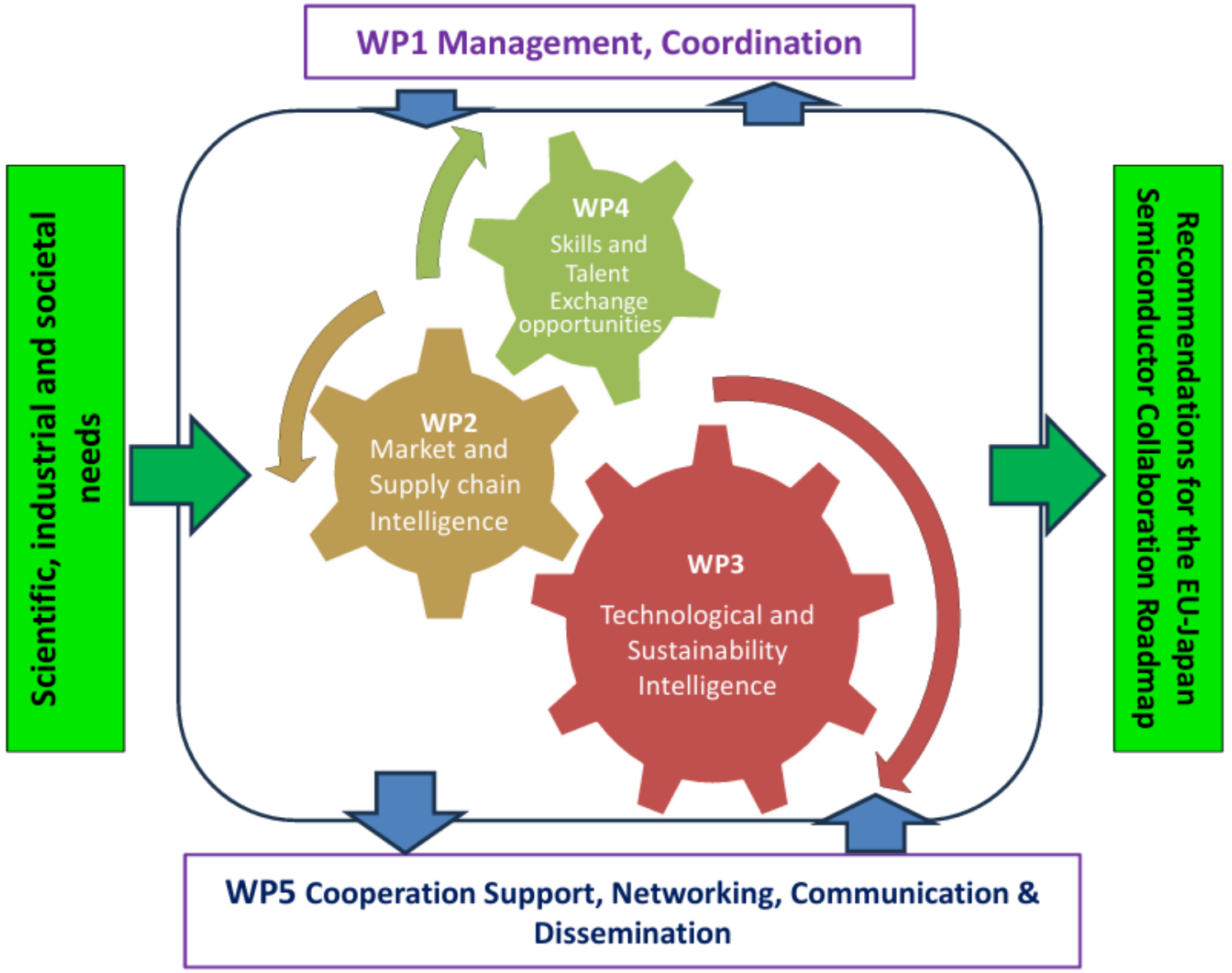
- i) **Advanced computing** (advanced nodes for logic and memories, in-memory computing, neuromorphic computing, quantum computing)
- ii) **Advanced functionalities** (power devices, RF devices, sensors, energy harvesting devices, semiconductor-based photonics devices)
- iii) **Ground breaking technologies/Beyond-CMOS** (2D materials and devices, CNT, spin devices, small slope switches, etc.)
- iv) **Heterogenous integration and packaging**
- v) **Sustainable materials, devices and manufacturing**

Possible Joint activities

- Webinars, Workshops in EU & Asia-Pacific & Online
- Contribution to Regional & International Technology Roadmaps (IRDS)
- International R&D&I cooperation on topics of mutual interests
- International Summer Schools & Training activities
- Exchange of researchers, Joint PhDs
- Access to Research Infrastructures
- Standardisation needs for emerging technologies
- Cooperation in the semiconductor value chain
- Position papers for future joint activities

JASMINE Horizon-Chips JU

Japan and EU Semiconductors: Mutual Innovation & Excellence



19 Partners, Europe & Japan, March 2026-August 2027

Challenges for the future

Great advances during the last century

- 100 years of the Field Effect Transistor (FET): The first concept of the FET was documented in a Canadian patent filed by *Julius Lilienfeld* on October 22, 1925 (publication: J.E. Lilienfield, U.S. Patent 1,745,175, 1930)

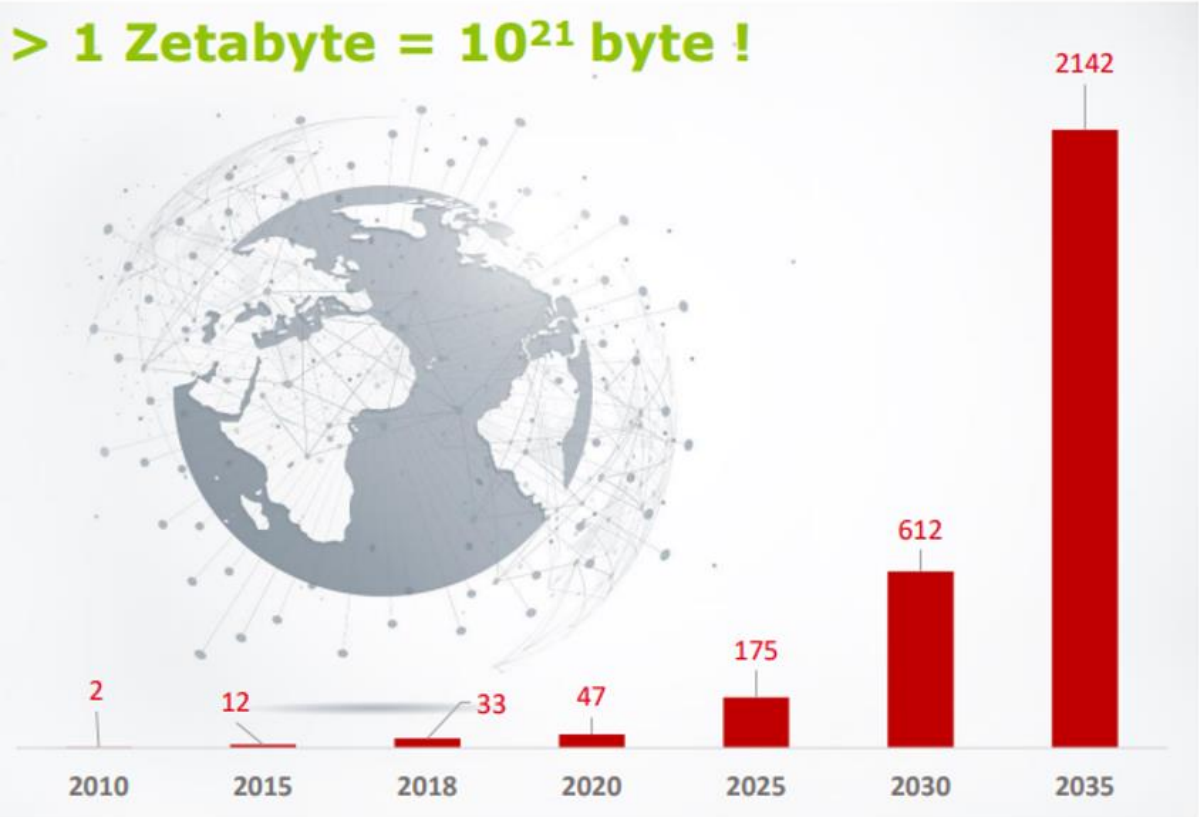
- 75th Anniversary of the 1st working Transistor, Nov. 1947 – Jan. 1948, *Walter Brattain, John Bardeen, William Shockley* (Nobel Prize in Physics in 1956)

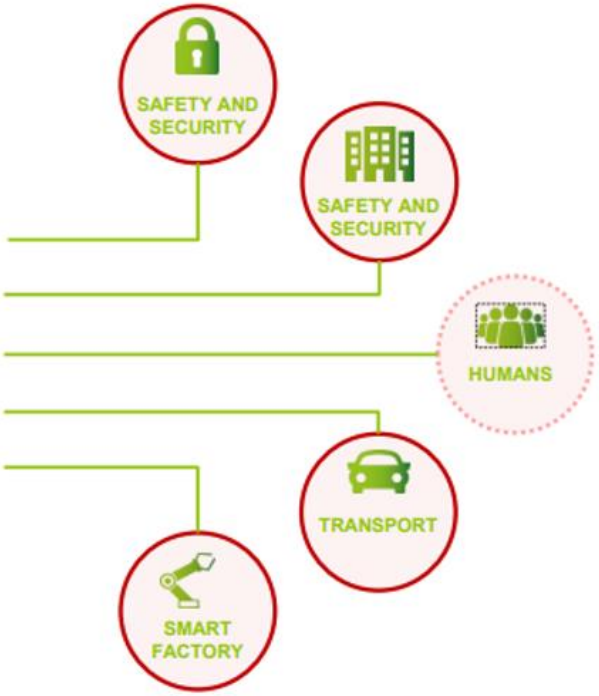
- 60th anniversary of Gordon Moore's prescient observation, in 2025, that became the catalyst for transistor scaling and the modern digital age : "Cramming more components onto integrated circuits" (*G.E. Moore*, Electronics, vol. 38, no. 8, 1965, pp. 114-117)

=> But, we are facing **substantial challenges** for the future electronic systems but **"There's still Plenty of Room at the Bottom**" (*Richard Feynman,* 1959) **for nanoscale structures**, and, in addition, **"There's Plenty of Room at the Top" for future 3D system integration**

Challenge: Data deluge

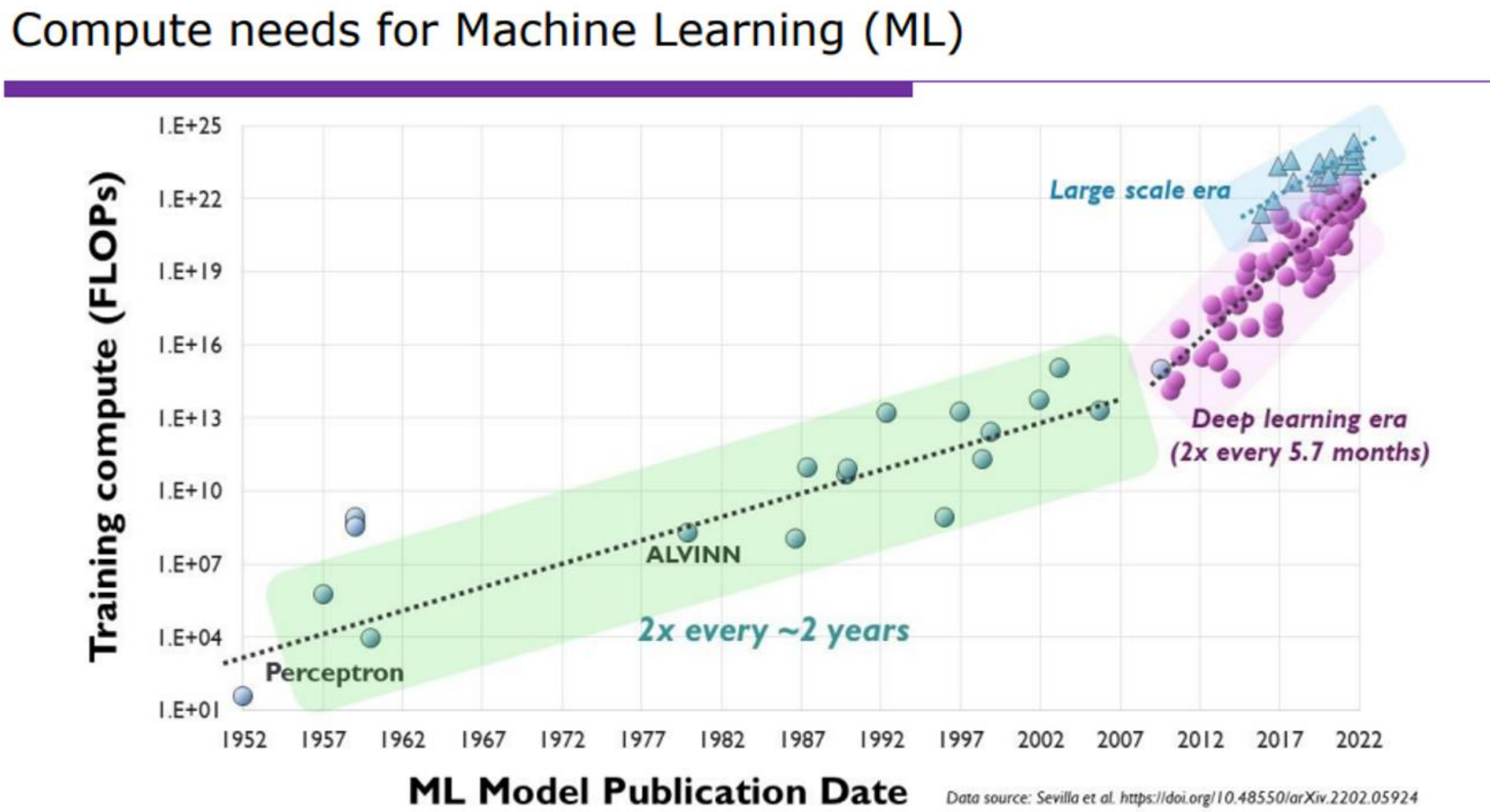
Global data generation



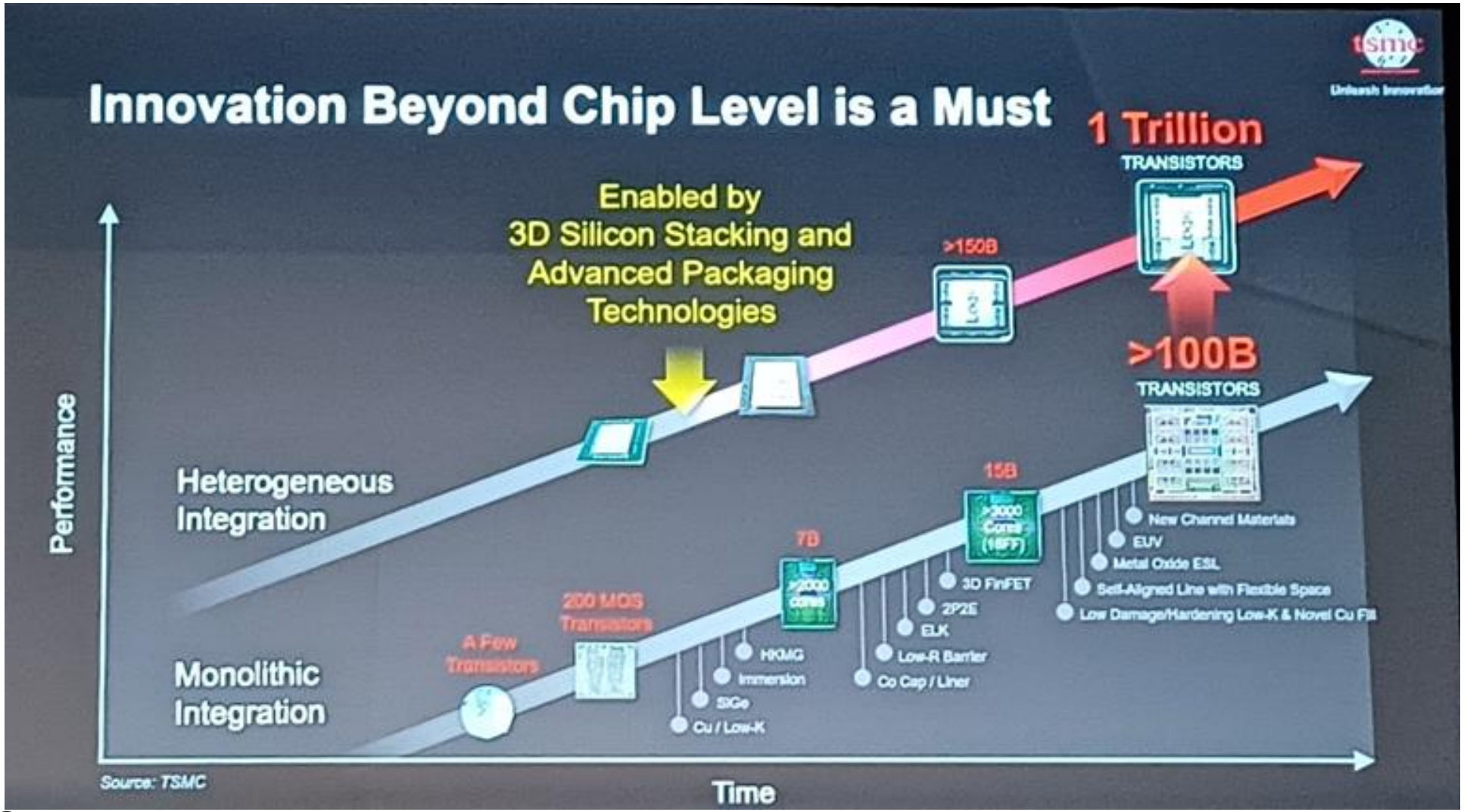


> A true data deluge, not only generated by humans!

Challenge: Computing needs



Challenge: Monolithic and Heterogeneous integration



Challenge: The required gain in energy efficiency

>1000x

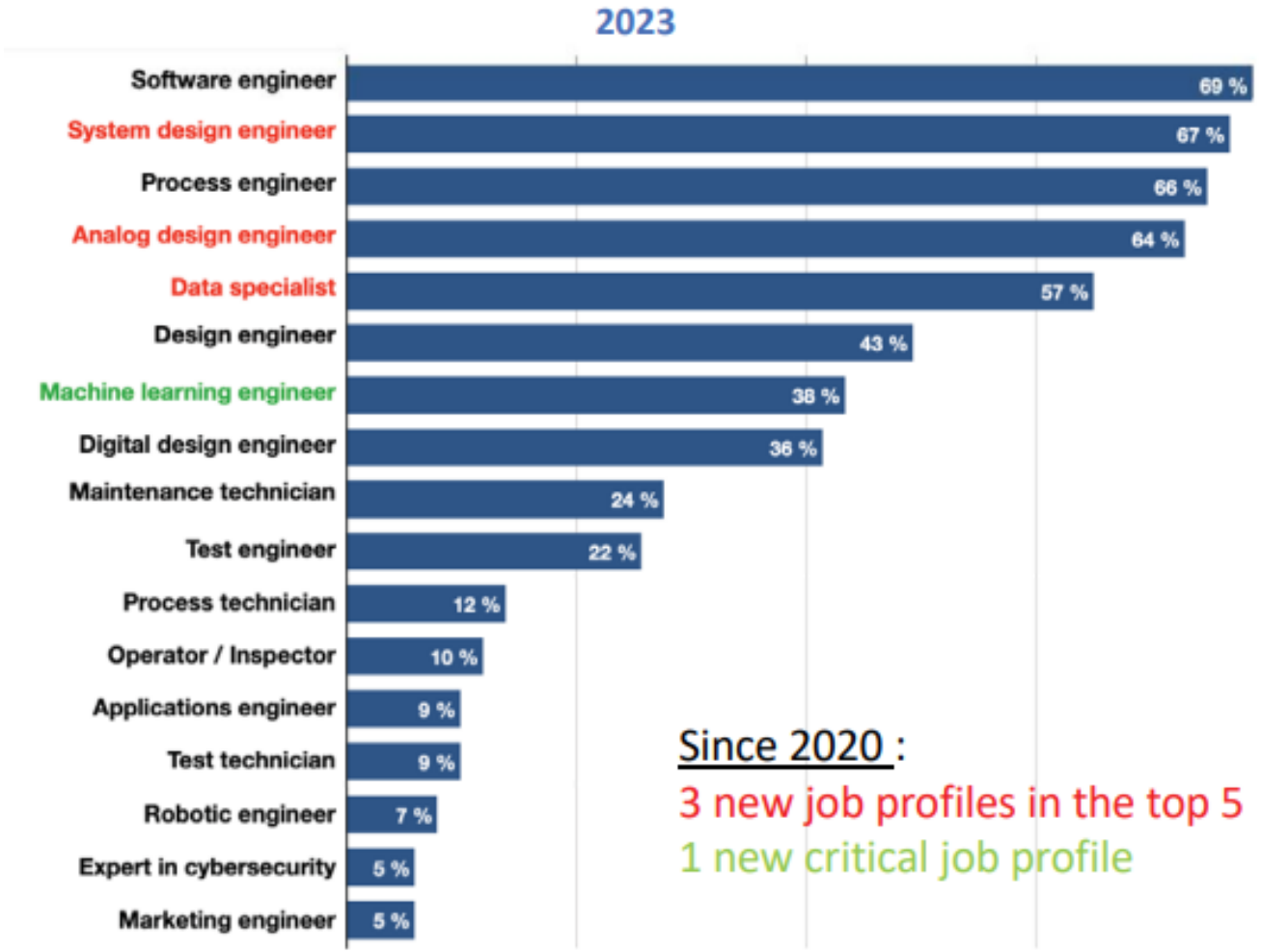
By the next decade

- CMOS scaling
- Memory technologies
- Disruptive Computing
- Chiplet & 3D System

Challenge: Complex supply & value chains

Source: DECISION Etudes & Conseil

Challenge: Skill shortage



Source: DECISION Etudes & Conseil

Projected semiconductor workforce gap:

- 2024-2030: **68,700 jobs** including :
  - ➢ 34 % of Technicians
  - ➢ 57 % of hardware engineers
  - ➢ 8 % of software engineers and data specialists
- This shortfall corresponds to 34 % of the overall industry demand,

⇒ The supply may cover only 66 % of the expected demand

Motivation & Objectives for International Cooperation

Motivation for International Cooperation in Semiconductors

- **Semiconductors & Semiconductor-based photonics** are pivotal technologies for almost all existing industrial sectors, as demonstrated by the recent chips shortages

- **International cooperation** is key for:

  -**knowledge** exchange

  -**speeding up** technological innovation (e.g. ITRS/IRDS, IPSR-I, ECS-SRIA, NEREID, SDRJ): computing needs, energy efficiency, advanced functionalities, heterogeneous integration

  -**addressing technological gaps**

  -**reducing cost** by avoiding duplicated research

  -**strengthening** complex **supply and value chains** (no region can cover the whole value chain)

  -manage **risks** due to the turbulent geopolitical context

  -is encouraged by the new **strategies** of leading semiconductor countries (**digital partnerships**)

  -overcoming **skill shortage**

  Source: DECISION Etudes & Conseil

  -gaps in **standardisation**

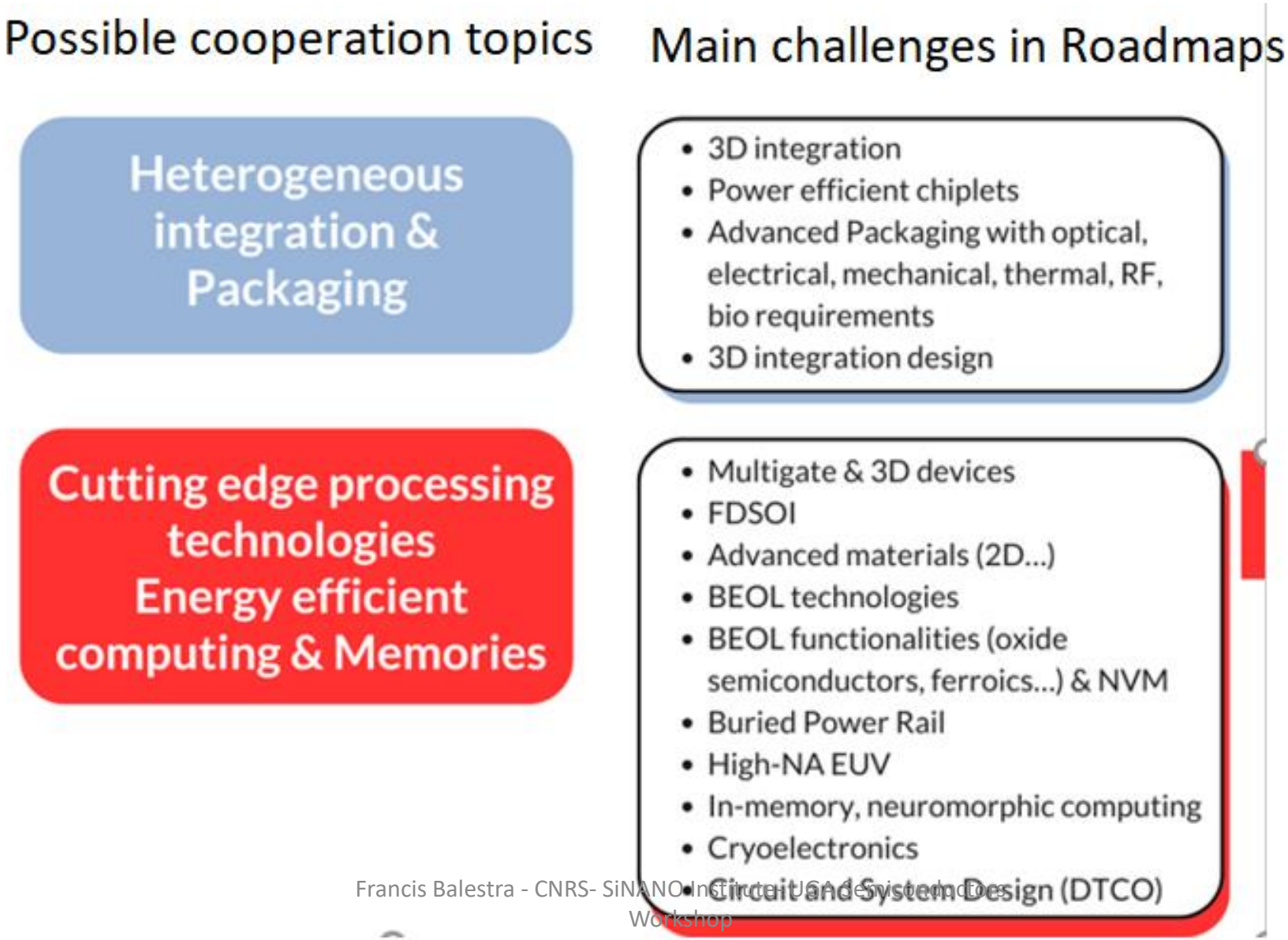
Objectives of International Cooperation in Semiconductors

- **To implement and strengthen the DPs**
- To build **balanced semiconductor partnerships** with like-minded countries
- To set out cooperative framework on **initiatives of mutual interest**
- To identify and support the establishment of the **most promising scientific international collaborations** and **to overcome the main challenges in the Roadmaps**
- **To consolidate sovereignty through skills**

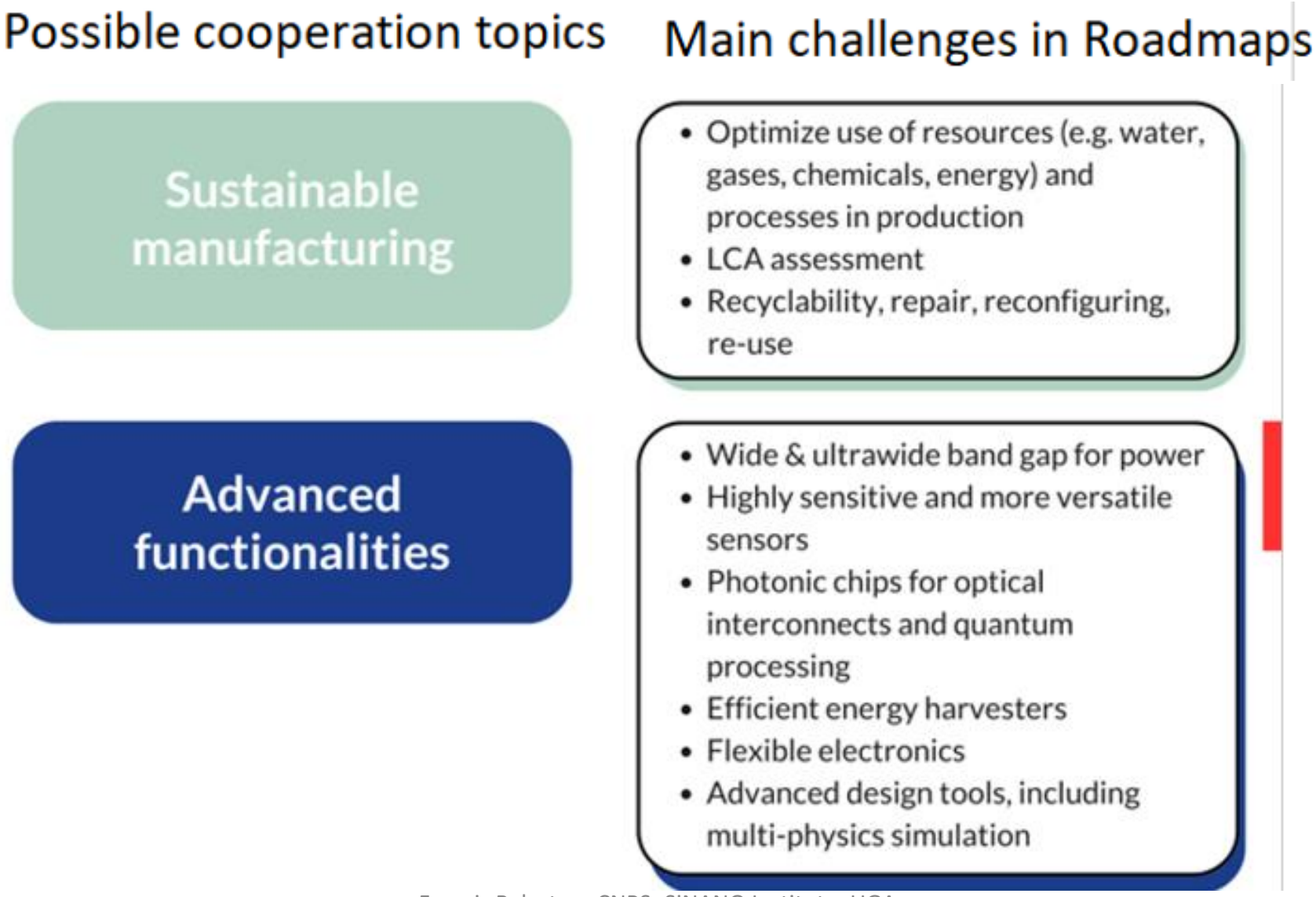
  =>*Skill Roadmap* aligned with Research and Industrial Roadmaps, Strengthen *scientific and technological competences* through international cooperation, Develop *students skills*, Attract *international students*
- To organize **matchmaking events**
- To support the growth of the **Semiconductor industry in growing markets** through **focused research alliances** based on awareness of advanced research activities
- To strengthen **Europe's and Partner Country's position** in emerging **technologies** and global **value chains** in this area and to contribute to the **Chips Act and Digital Agenda**

Possible cooperation topics

Possible science and technology cooperation

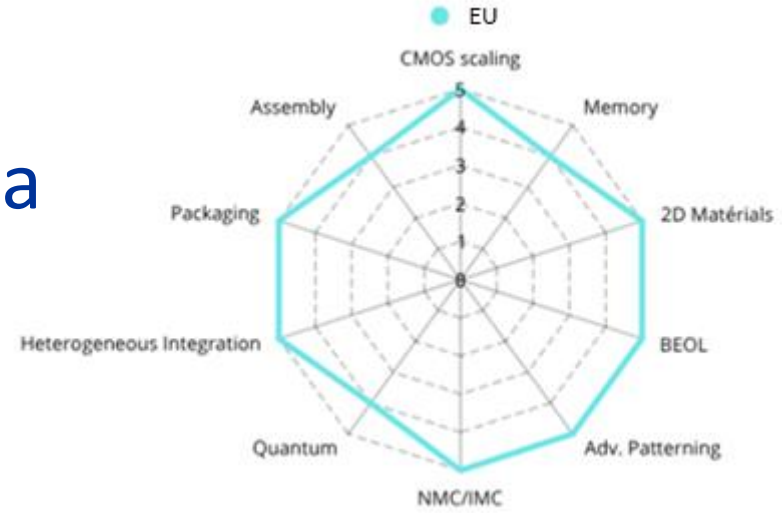


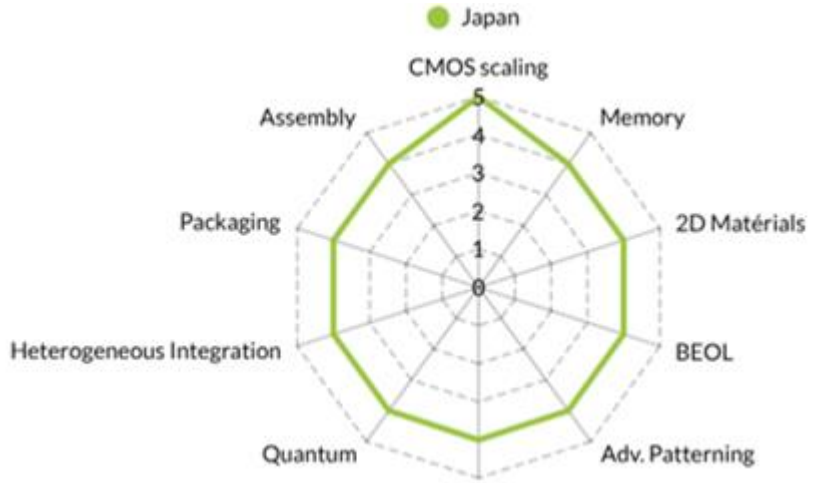
Possible science and technology cooperation



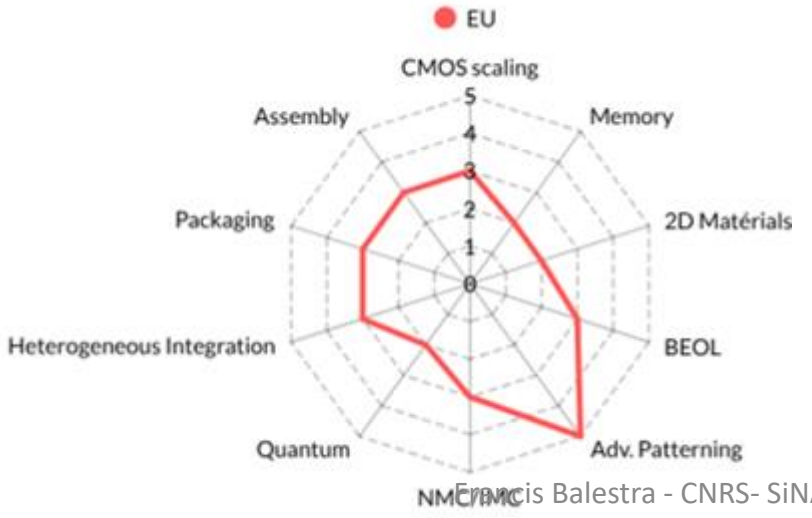
Involvement of RTOs/Academia & Industry for Advanced Computing Technologies => Possible cooperation

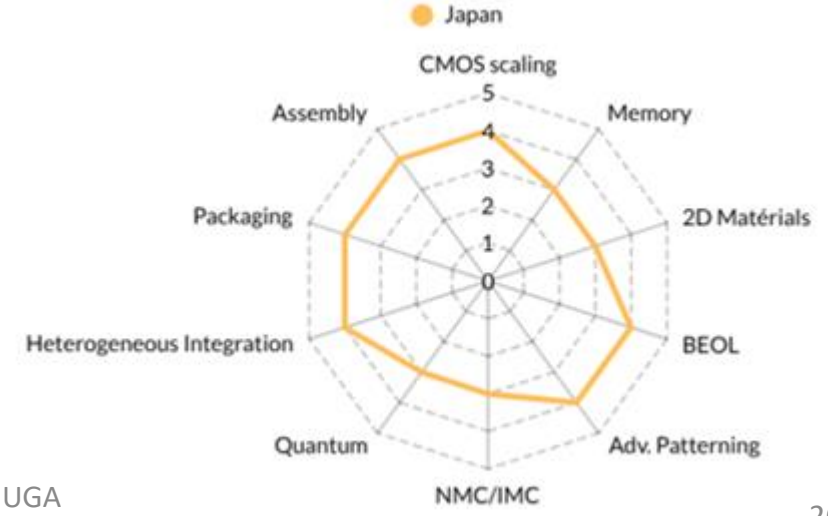
RTOs/Academia



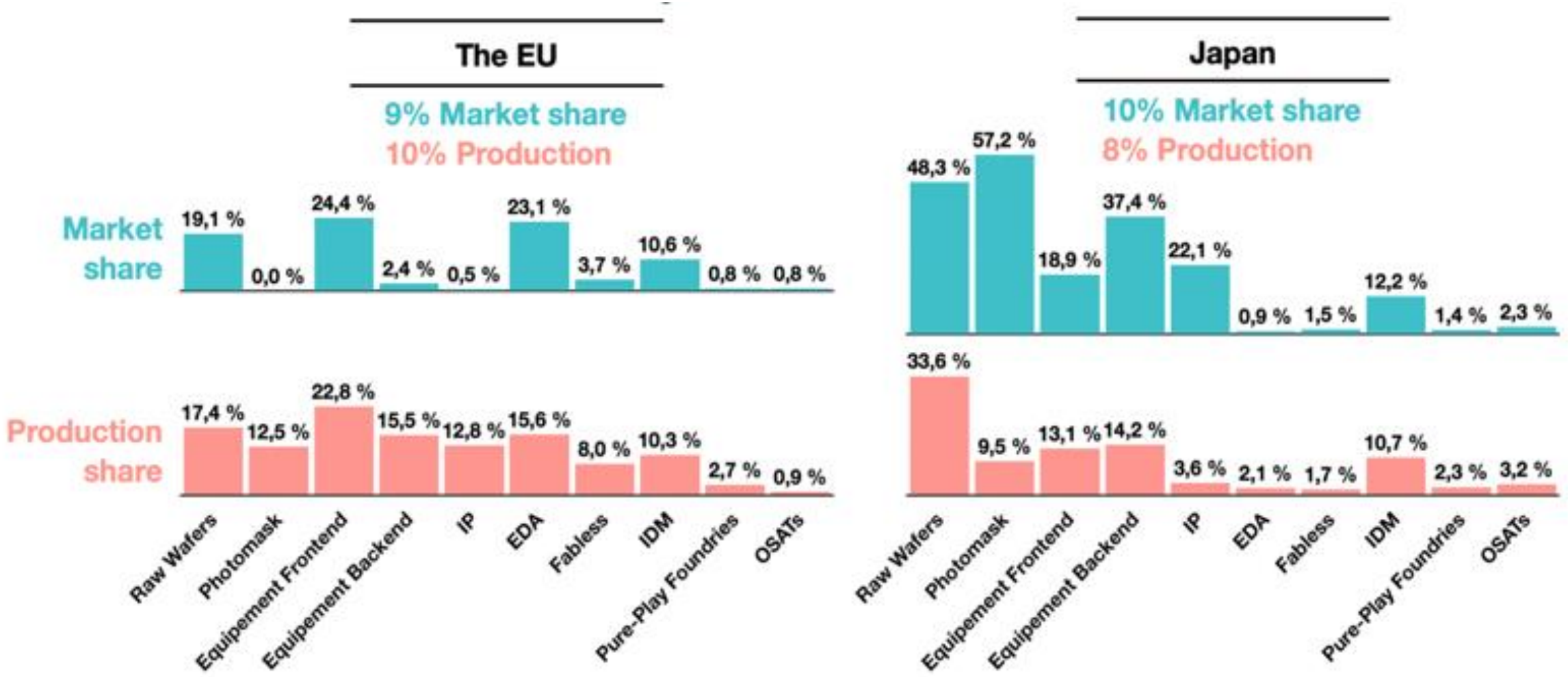


Industry

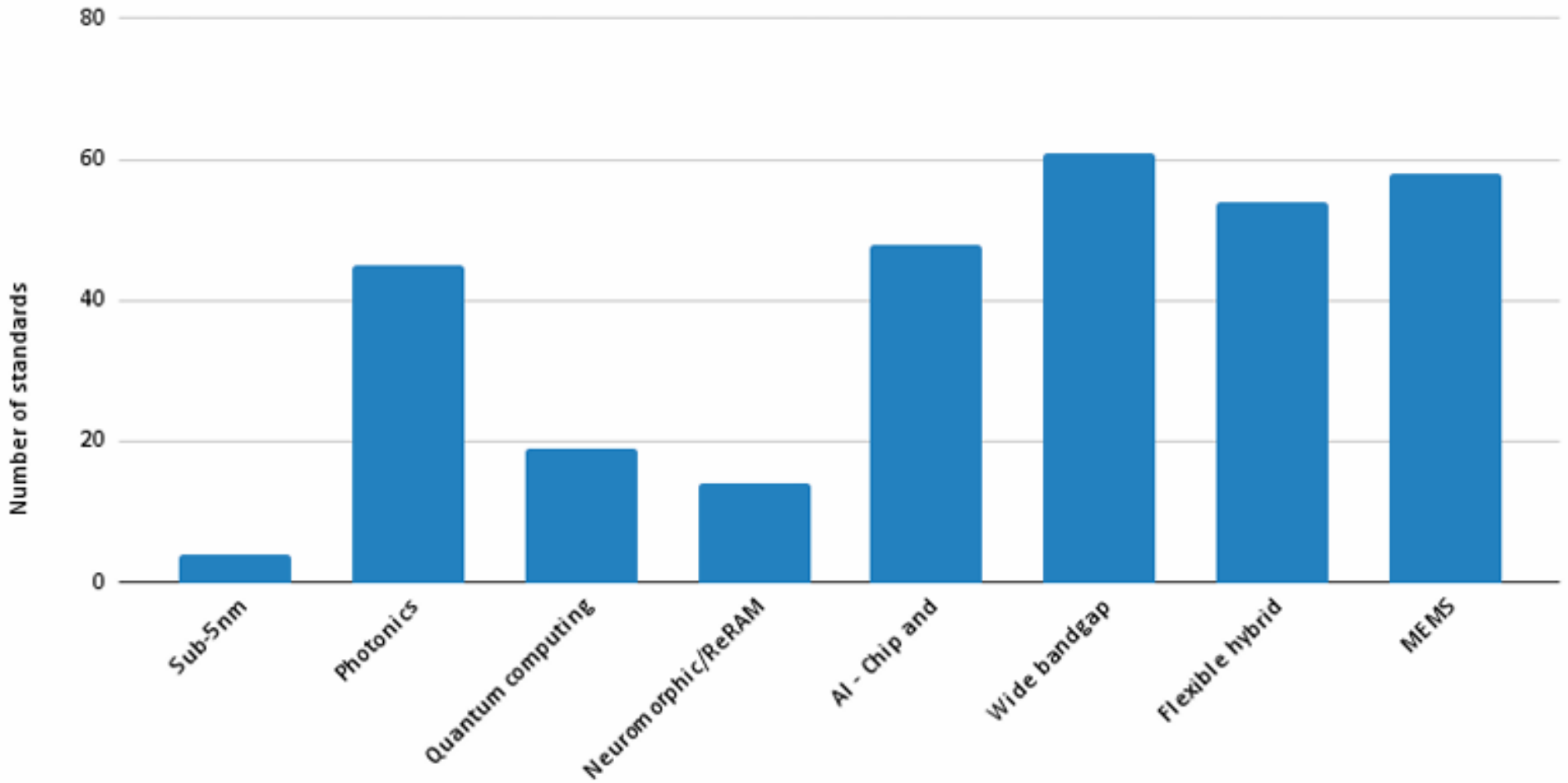




Market & Production shares in the value chain
=> Possible future cooperation topics in the value chain



Number of standards vs Category modules or Components => Possible cooperation



THANK YOU FOR YOUR ATTENTION!

The EU-Japan Digital Week is an initiative under the EU-Japan Digital Partnership and is supported by the following projects and organisations

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ETSI

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TAKING EUROPEAN INNOVATION GLOBAL

INPACE
Indo-Pacific-European Hub for Digital Partnerships

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