Low Power Nonvolatile NBFPGA for Space and Cryogenic Applications

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NBFPGA :
NanoBridge Field-programmable gate array

Outline

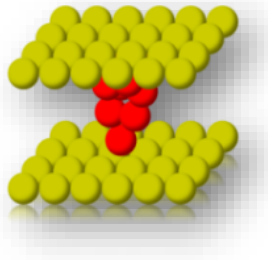
What is NanoBridge ?

NanoBridge FPGA

- Space application
- Cryogenic application
  ~ Quantum controller

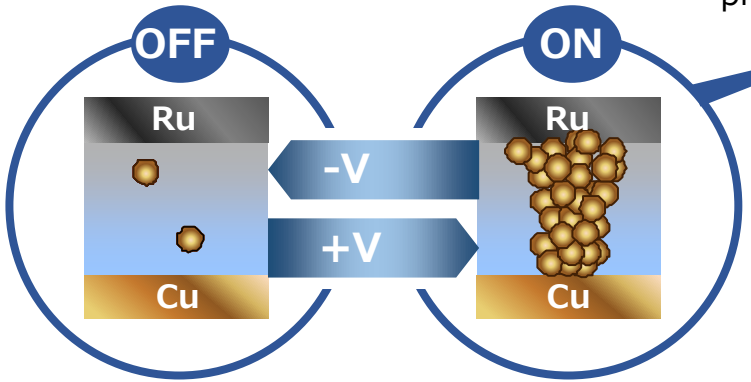
Conclusions

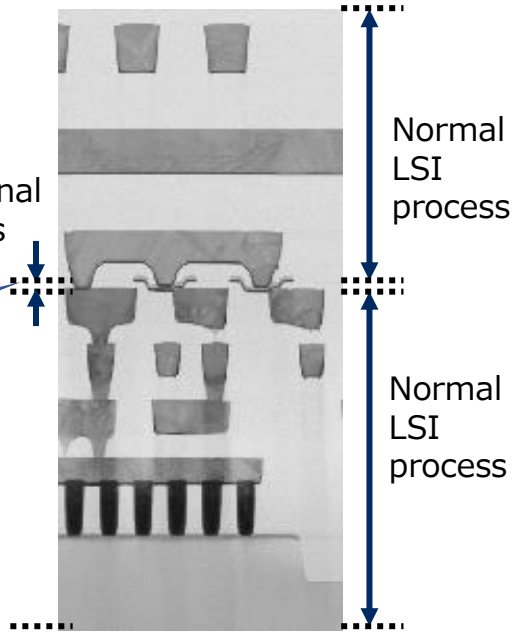
Atom switch : general name
NanoBridge（NB）: trademark



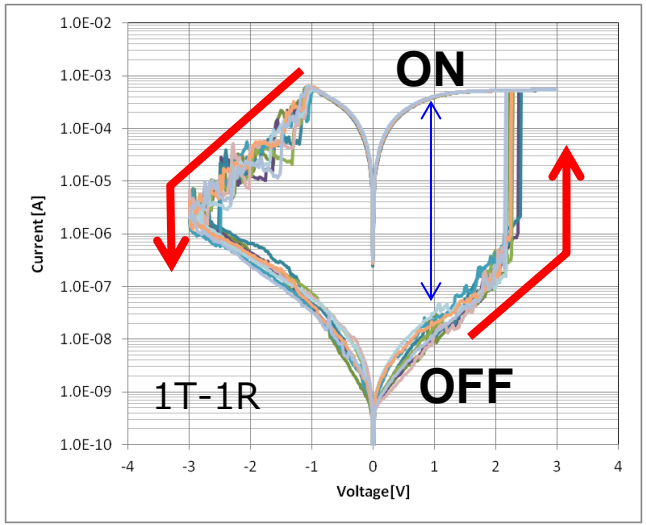
What is NanoBridge ?

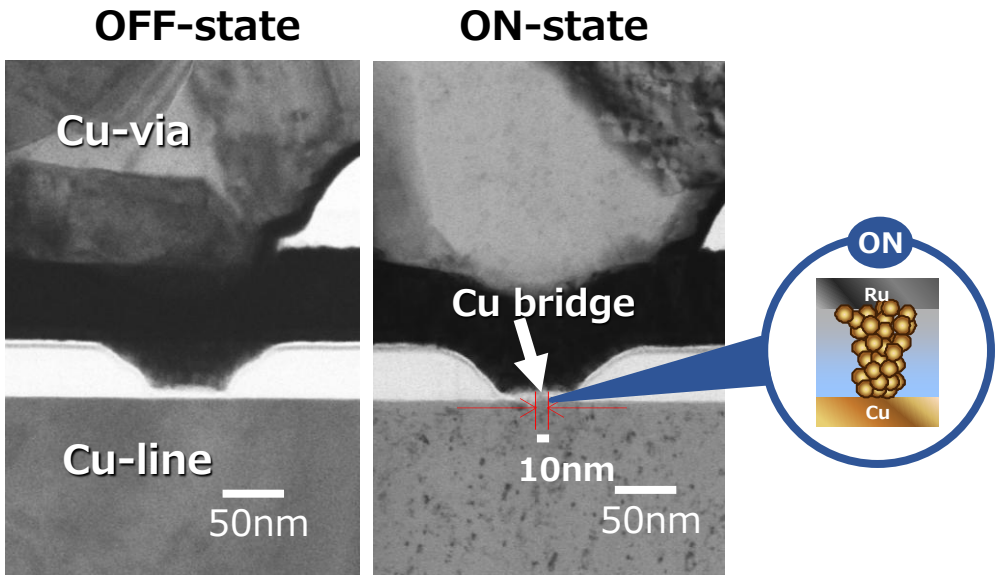
- Reprogrammable, Nonvolatile, Small metal switch →Rad-hard, Low-power
- ON/OFF switching by applied voltage
- Manufactured in a semiconductor fab with only two additional masks
- Application:
  1. Routing Switch for Field Programmable Gate Array (FPGA)
  2. Nonvolatile Memory





NanoBridge I-V curves

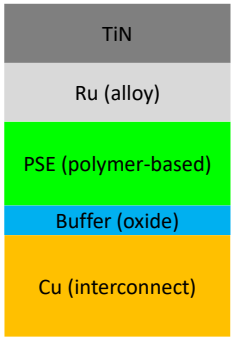


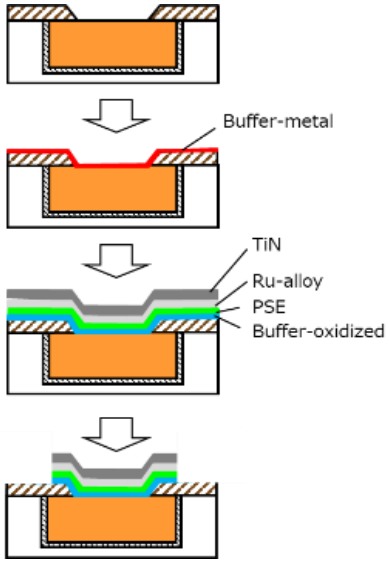


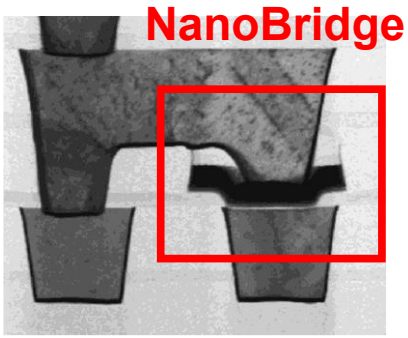
M. Tada et al., IEDM 2010

Key process technology of NanoBridge Integration

- The copper wiring itself is used as the active electrode of the NanoBridge.
- The upper and lower electrodes are physically separated, so there is no short circuit during processing.

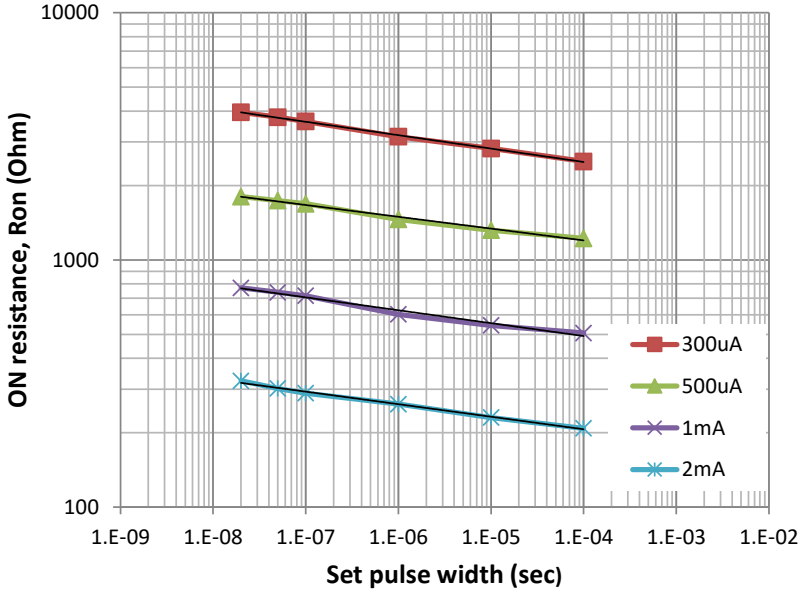




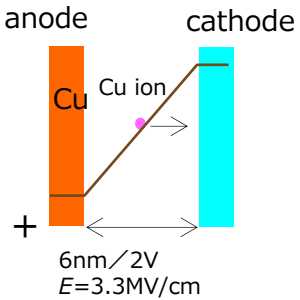


M. Tada et al., IEDM 2009

Modified Faraday's law



$$R = Z' \cdot I^{m} \cdot t^{n}$$



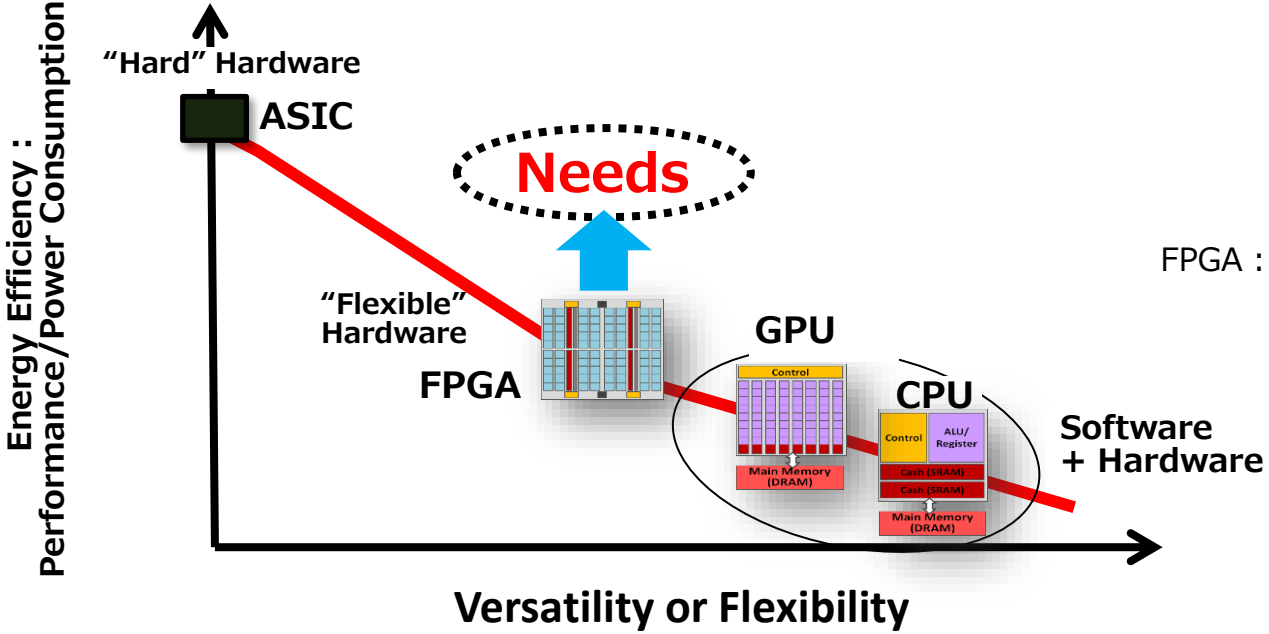
$m = -1.31$ and $n = -0.05$

M. Tada et al., IEEE TED 2017
M. Tada, IEEE IRPS 2022 (Invited)

NanoBridge FPGA

FPGA position

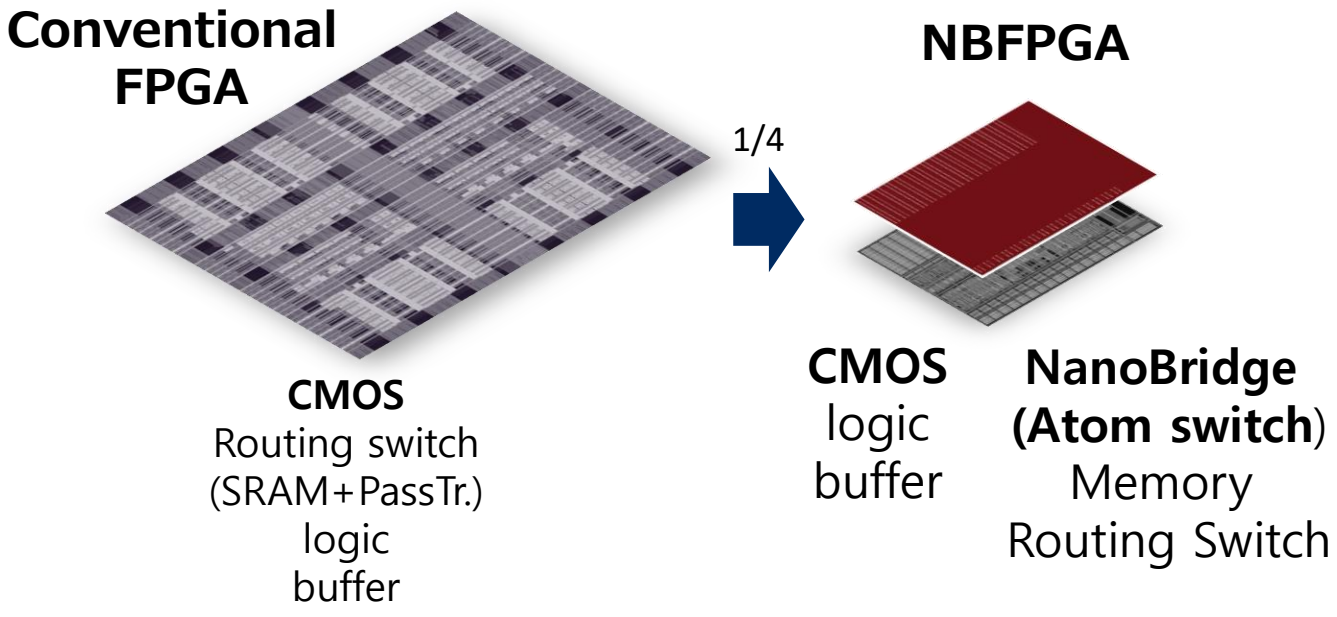
- For logic chips in IoT, programmability for functionality updates is essential.
- Compared to CPUs and GPUs, FPGAs are the best choice due to their superior energy efficiency despite offering similar programmability.



FPGA : Field Programmable Gate Array

Concept of NanoBridge-FPGA

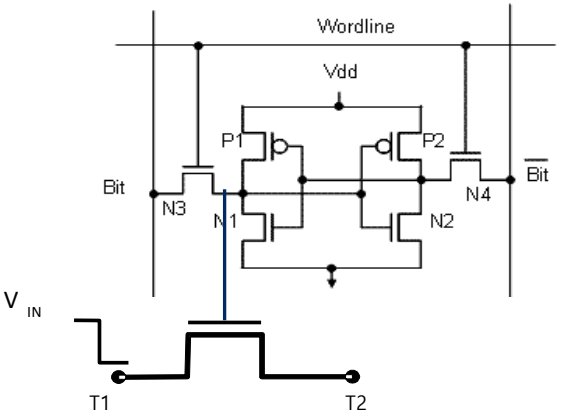
- **Conventional FPGA is composed of volatile switch of SRAM and PassTr, which occupies large chip area.**
- **NanoBridge replaces the SRAM and PassTr. in routing switch for low-power FPGA.**



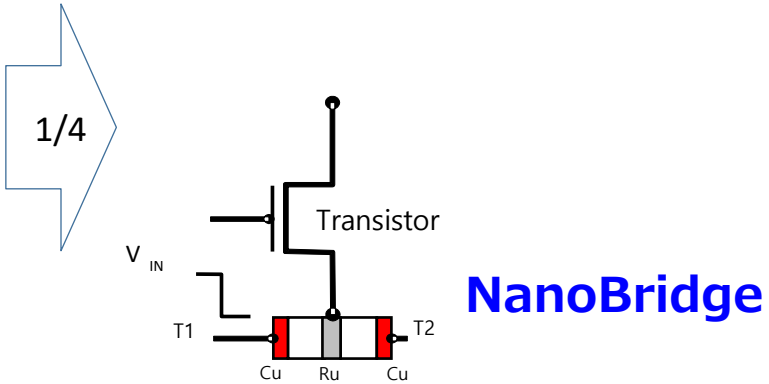
Switch element

NanoBridge replaces SRAM and Pass-transistor in routing switch for low-power FPGA.

Conventional FPGA



NBFPGA

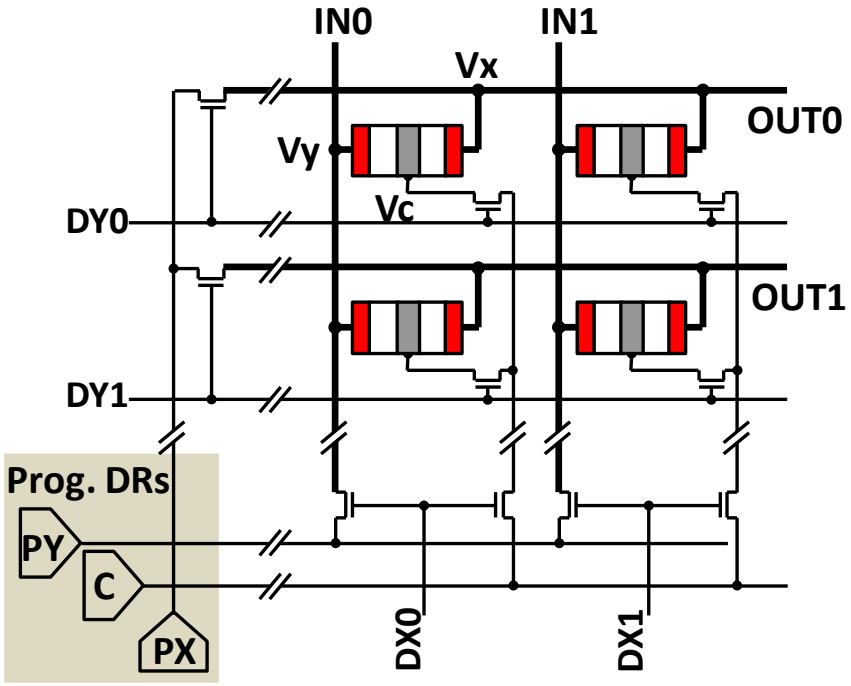


6T-SRAM+PassTr.

1T2R:Complementary atom switch (CAS)

M. Tada et al., IEEE IEDM 2011

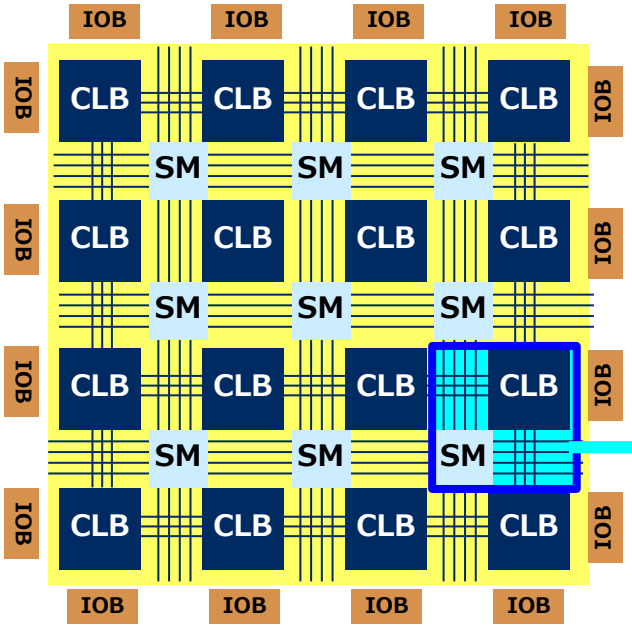
Crossbar switch



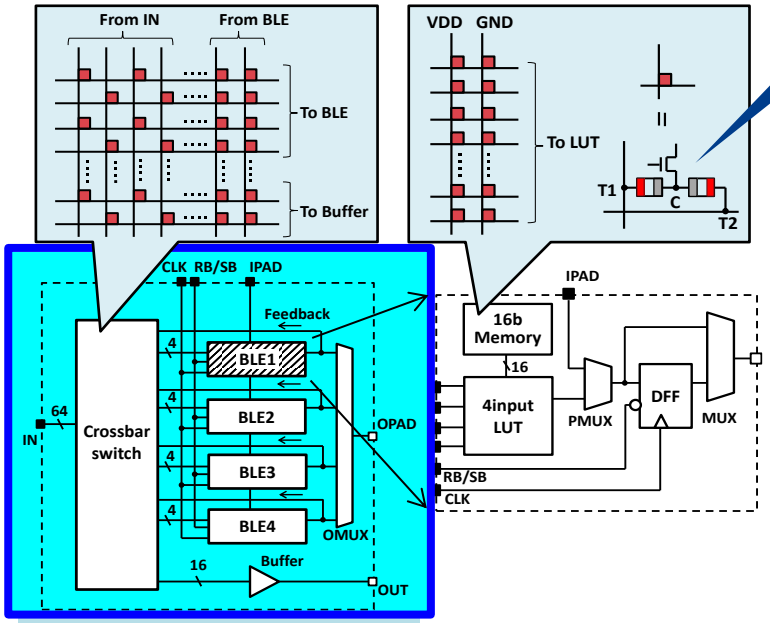
M. Miyamura et al., IEEE ISQED 2012

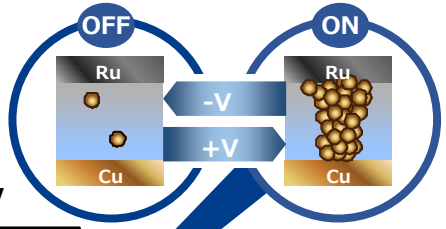
NB-based Configurable Logic Block

Standard FPGA design



NBFPGA design





NanoBridge

M. Miyamura et al., IEEE ISQED 2012

Demonstration of low-power operation（65nm）

Power is reduced to 1/7～1/20 for IoT applications.

2-1. NB-FPGA[NBS6500]とA社製CPLDの比較から
NB-FPGAは、同程度規模のCPLDの約１／7の消費電力で動作できる。

FPGA内の論理回路における動作範囲(動作率)を変えて、消費電力を比較した。
消費電力比：NBS6500/CPLD ≒ 1/7 ～ 1/20 となった。

NBS

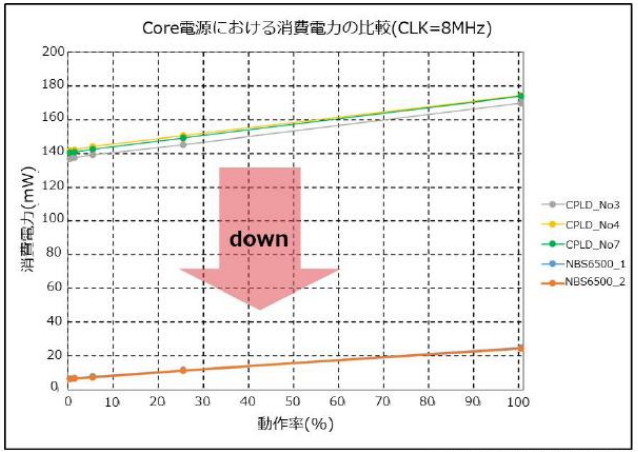
NBS6500	
4入力LUT数	8,448
Flip Flop数	8,448
Block RAM数	96
トータルSRAMサイズ(kb)	384
CLK系統	2
最大ユーザIO	128
Technology	65nm

Intel
(Altera)

A社製CPLD	
Logic Element (LE)	8,000
M9K Memory (Kb)	378
User Flash Memory (Kb)[2]	1,376
PLL	2
GPIO	250
Technology	55nm

搭載FPGA： NBS社製 NBS6500
A社製 CPLD

デモ機試作ボード



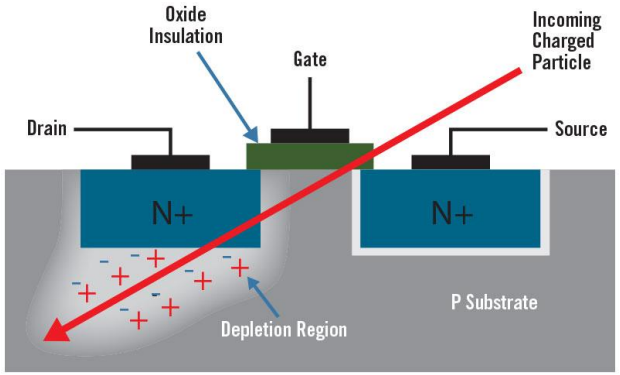
ET&IoT 2020 資料から更新

Courtesy of NEC Platforms, Ltd., DFS2020

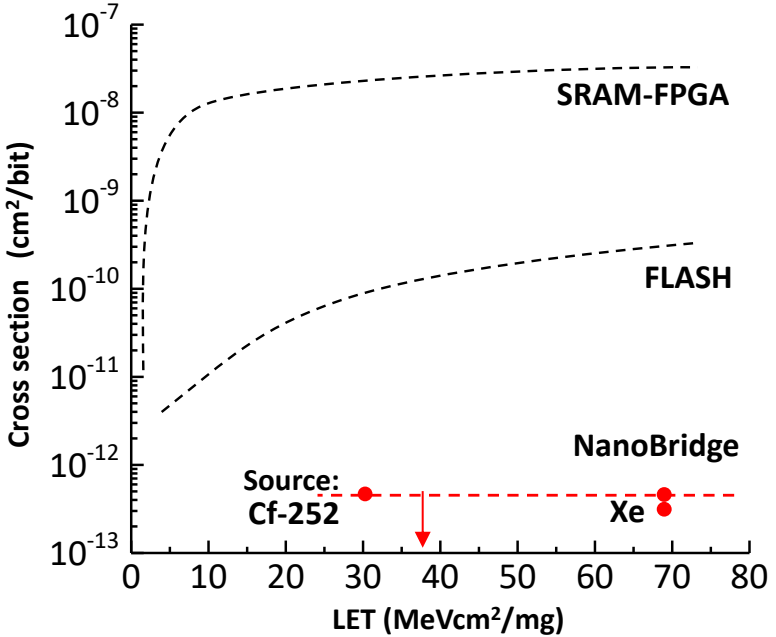
Space Application

Soft error : Cross Section of Single Event Upset

- SEU in NBFPGA has not been observed yet.
- Broken lines for SRAM, Flash FPGA are typical data quoted academic papers.



Single event upset



K. Takeuchi, JAXA the 29th Microelectronics workshop 2016

Demonstration of radiation resistance（1st generation）

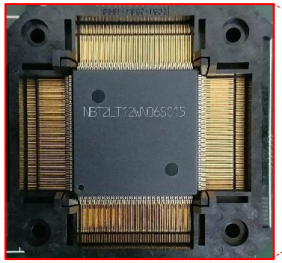
- Demonstration of radiation tolerance of NanoBridge FPGA
- Free from Single event upset (SET), Total ion dose effect (TID), Displacement damage dose (DDD)

Effect	Radiation	Source	Energy	Dose	DUT	Active	Judge
SEU	Neutron	Acc./Be	2MeV	3.6e11	NB-FPGA	Dynamic	OK
SEU	Neutron	Acc./Be	2MeV	1.2e12	NB-FPGA	Static	OK
SEU	Heavy Ion	Cf-252	30 MeV/cm²/mg	2.7e5	NB-FPGA	Dynamic	OK
SEU	Heavy Ion	Acc. /Xe	68.9 MeV/cm²/mg	2e7	NB-FPGA	Dynamic	OK
SEU	α-ray	Am	5.4MeV	1.1e8	NB-FPGA	Dynamic	OK
TID	Gamma-ray	Co60	1MeV	5kGy	AtomSW	Static	OK
TID	Gamma-ray	Co60	1MeV	5kGy	NB-FPGA	Dynamic	OK
DDD	Neutron	Nuclear reactor	<2MeV	1e14	AtomSW	Static	OK

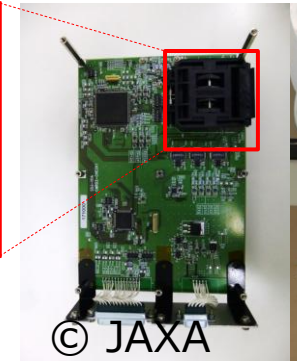
Sakamoto, MEMRISYS 2021, Courtesy of JAXA and KEK

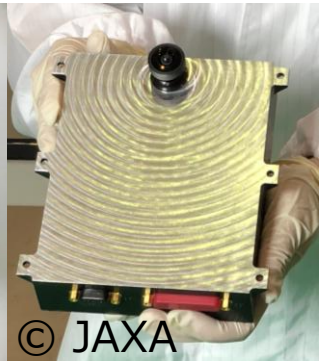
Highly radiation-hardened chip on JAXA satellite

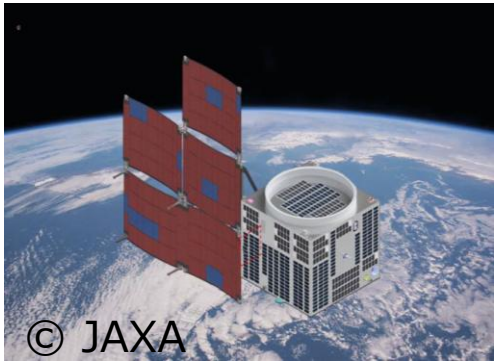
- On January 18, 2019, Japan Aerospace Exploration Agency (JAXA) launched the "RAPid Innovative payload demonstration Satelite-1 (RAPIS-1)," equipped with NEC's newly developed NBFPGA, on the fourth Epsilon Launch Vehicle (Epsilon-4) under JAXA's innovative satellite technology demonstration program.
- JAXA and NEC are now starting joint collection and evaluation of basic data on the NBFPGA, including error rate measurement, in a space In addition, the reliable operation of image data compression is also being verified.



NBFPGA







https://www.nec.com/en/press/201901/global_20190118_01.html

NBS6500 Overviews

Costumer sample NBT6500 series die

- Nonvolatile and reprogrammable
- Radiation tolerant to GEO and beyond

Non hermetic, QFP

Robust TID, 200krad (Co60)

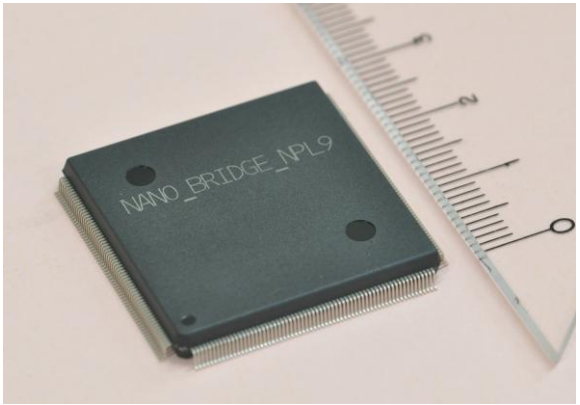
No configuration upset

- LET 68.9MeV-cm^2/mg

Protected SEU in Flip-flop

Next Schedule

- Program environment will be released for designated customers in 2023.



M. Tada et al., MEWS36, 2023

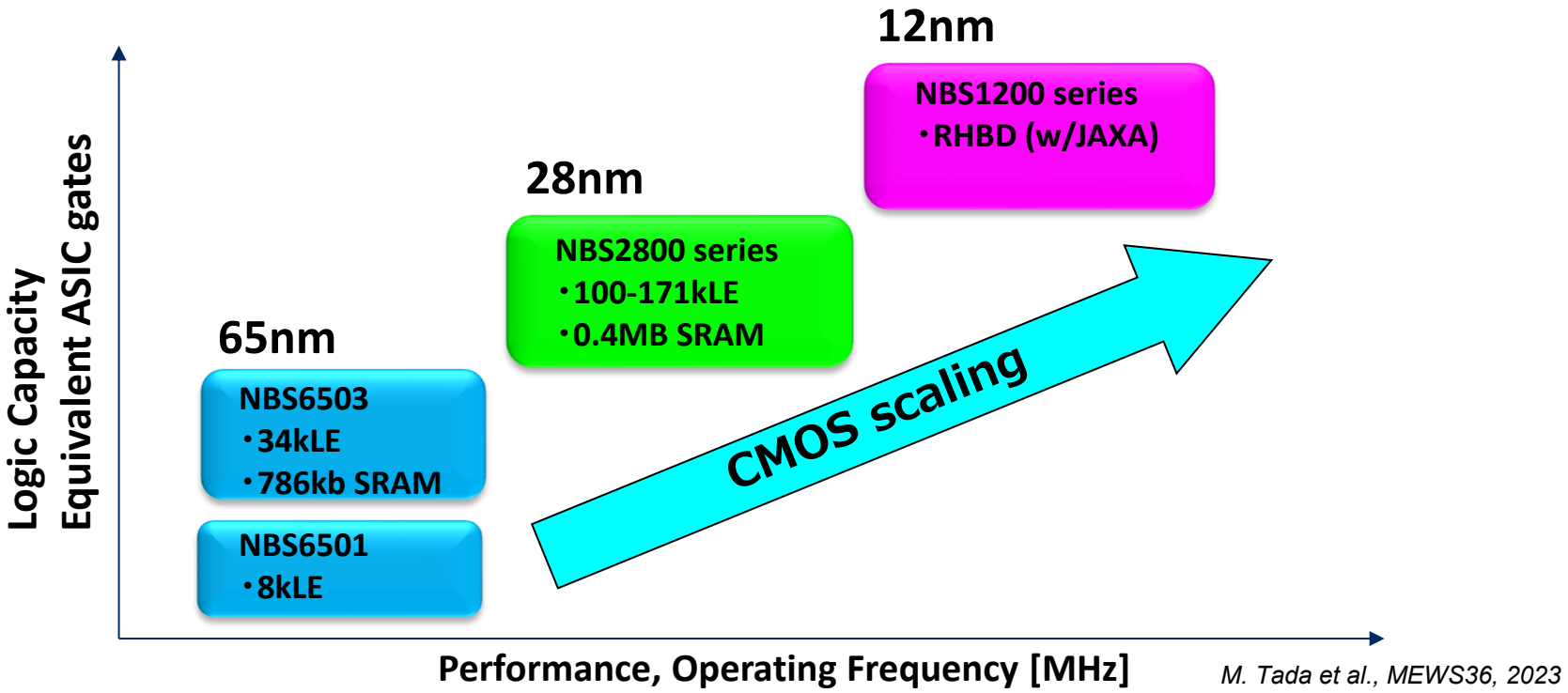
NBS6500 specifications

	NBS6501	NBS6503H
Technology	65nm	65nm
# of LUT	8,448	33,792
# of FF	8,448	33,792
	Dice type	Dice type
BRAM(bit/word)	8bitx512word	8bitx512word
SRAM type	Two Port	Two Port
# of BRAM block	96	384
# of CLK	2	8
GPIO	89	227
Core Voltage	1.2V	1.2V
IO Voltage	2.5V	3.3V
		5V tolerant
Operation frequency	100MHz	100MHz
Package	LQFP100/QFP208	C-QFP256

M. Tada et al., MEWS36, 2023

NBFPGA Families Plan

NBFPGA is looking ahead for larger capacity of FPGA with rad-hard.

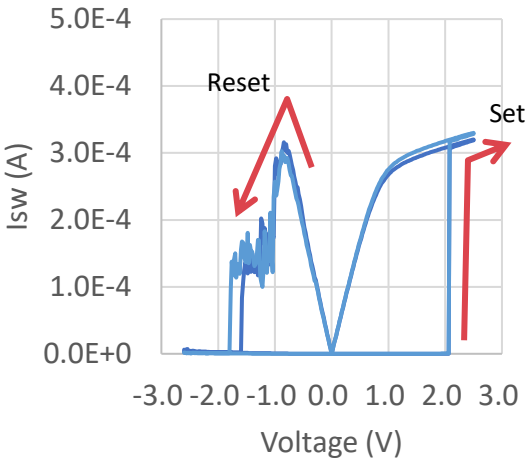


M. Tada et al., MEWS36, 2023

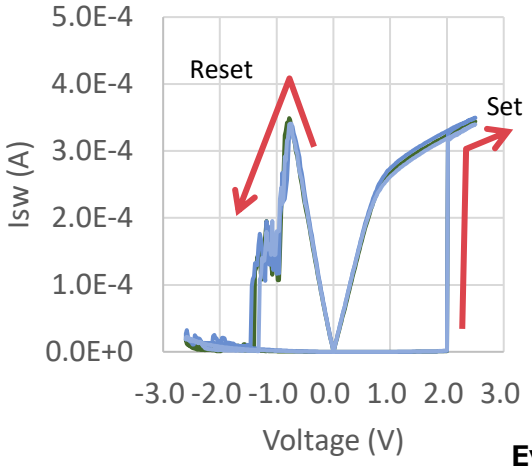
NanoBridge Characteristics

Fundamental NanoBridge programming is confirmed irrespective of CMOS technology node.

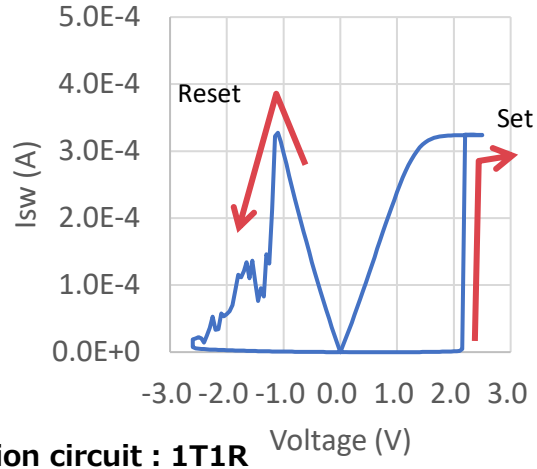
65nm



28nm

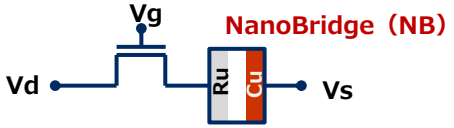


12nm



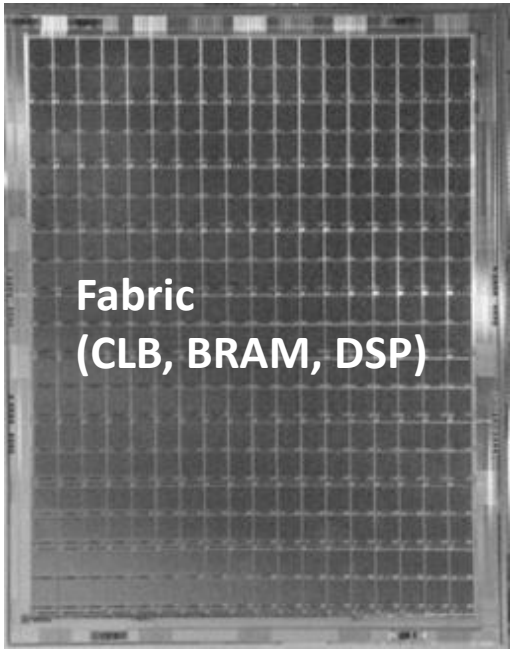
M. Tada et al., MEWS36, 2023

Evaluation circuit : 1T1R

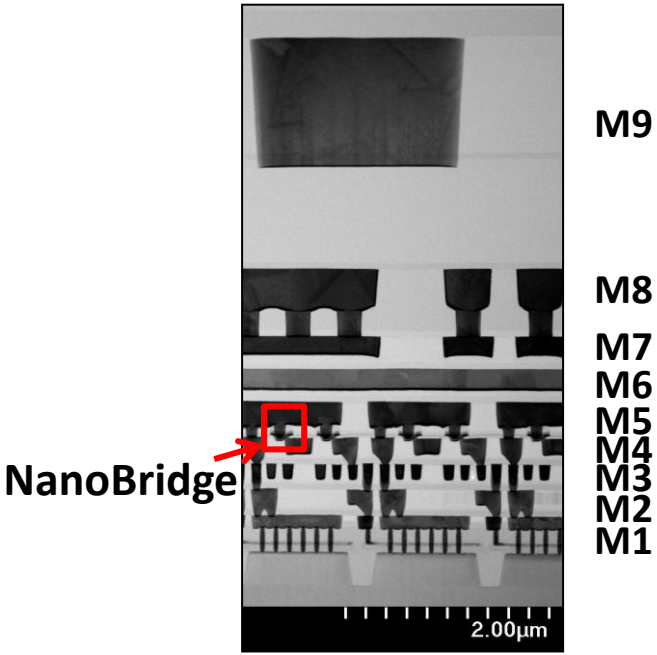


NBS2800 series

Largest number of LUTs among FPGAs using novel nonvolatile memories and switches



28nm-node

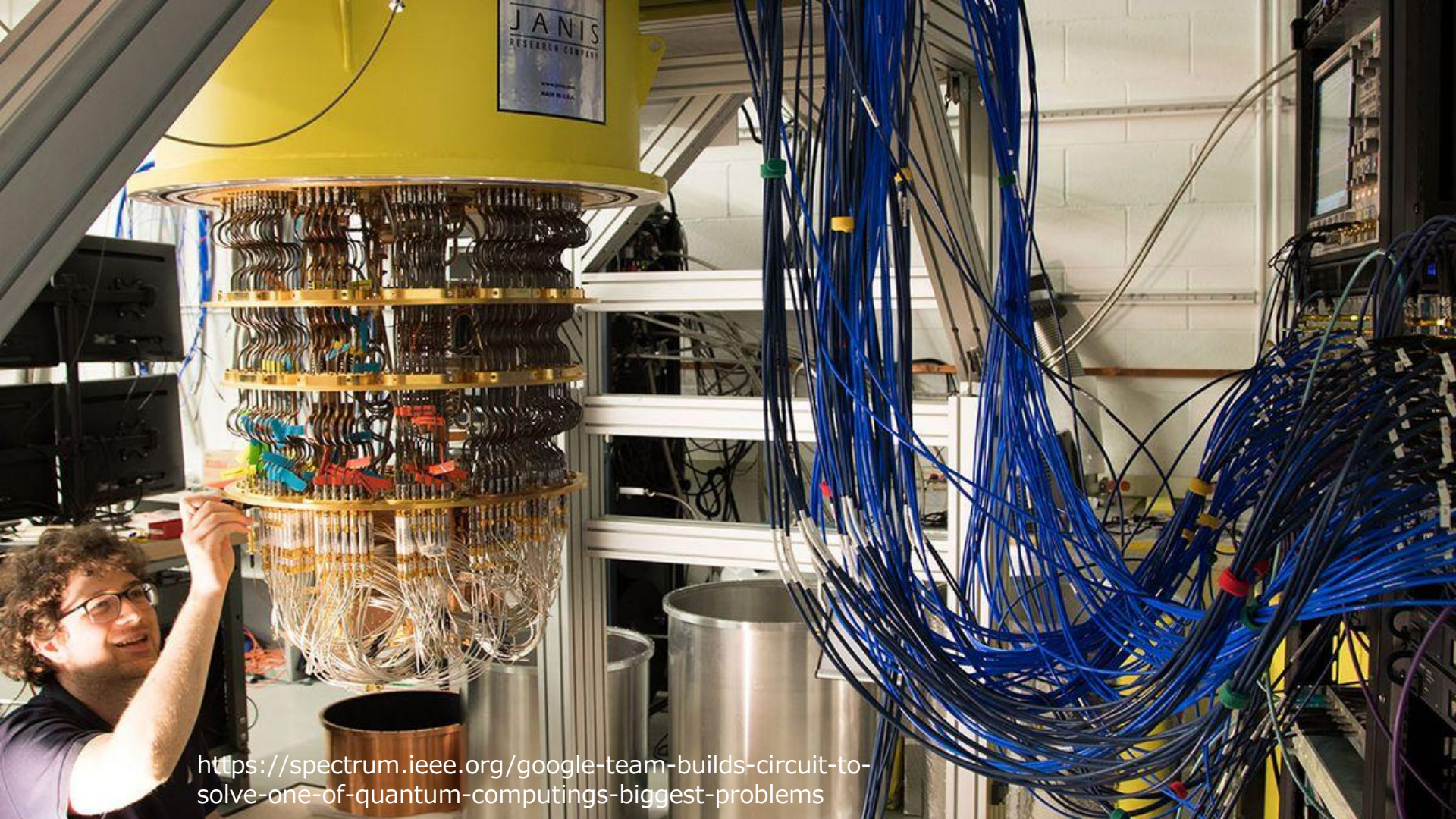


R. Nebashi et al., FPL 2020

Technology node	28nm 1P9M
# of LUTs	171k
# of NBs	173 Mb
Block RAM	3.2 Mb
PLL	5
DSP	648
FPU	2
GPIO	240
LVDS	16
Core voltage	1.05 V
IO voltage	1.8 V

Cryogenic application

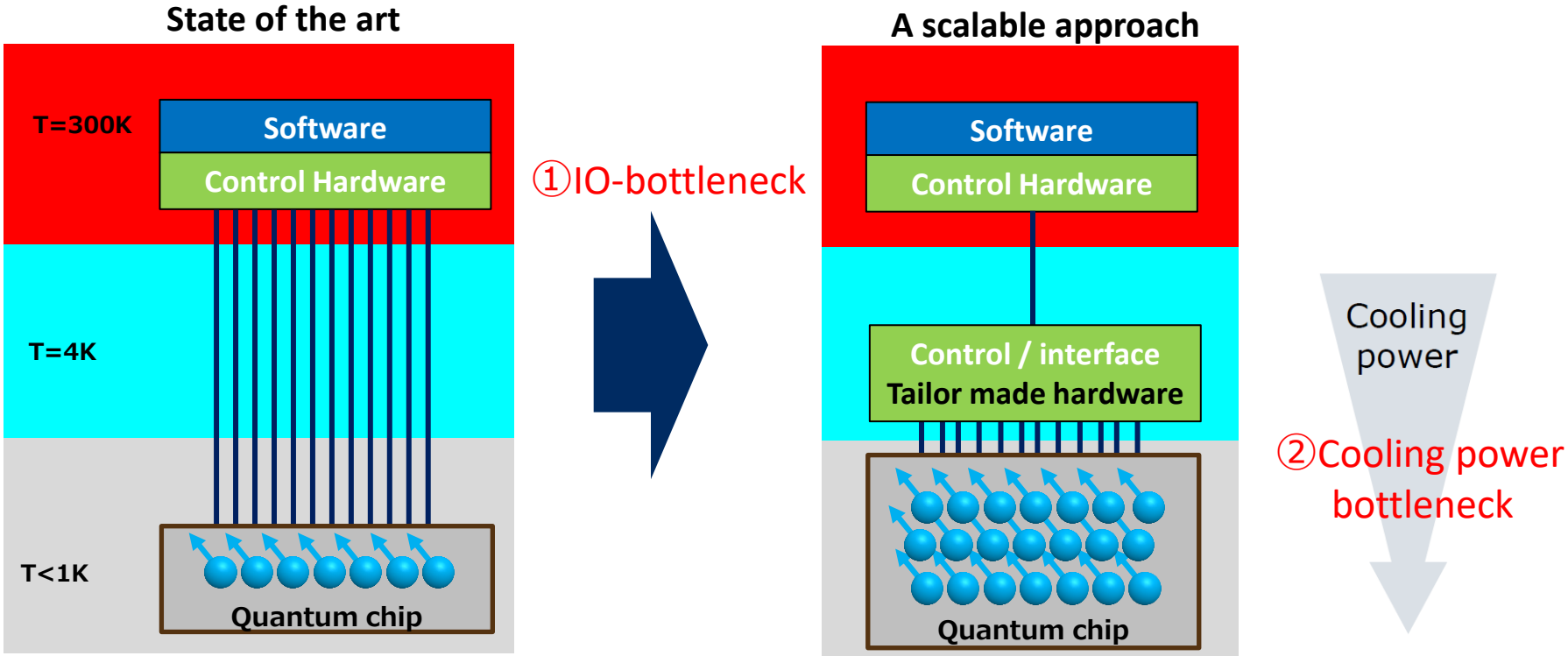
~Quantum controller~



https://spectrum.ieee.org/google-team-builds-circuit-to-solve-one-of-quantum-computings-biggest-problems

How to scale qubit

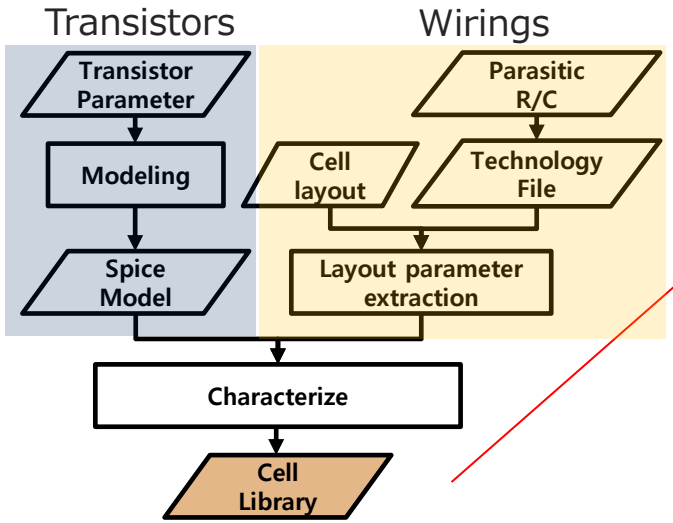
- Challenge : Cables expensive, heavy, too big, not scale
- Challenge : Limited cooling power



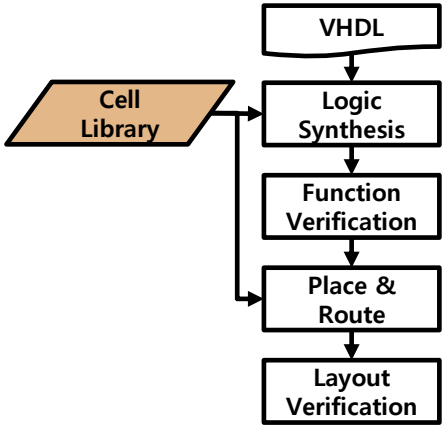
Standard cell library for cryo-CMOS circuits

- **Cell library construction consists of**
  - **Measurements of electrical properties of transistors and wirings at 4 K**
  - **Extraction of parameters and modelling**
- **We used technology nodes of 65 nm (core voltage 1.2 V/ IO voltage 2.5 V)**

K. Okamoto et al., 2022 IEEE International Interconnect Technology Conference, IITC 2022 (pp. 139-141),
M. Tada *et al.*, "*IEEE Journal of the Electron Devices Society*, vol. 12, pp. 28-33, 2024.



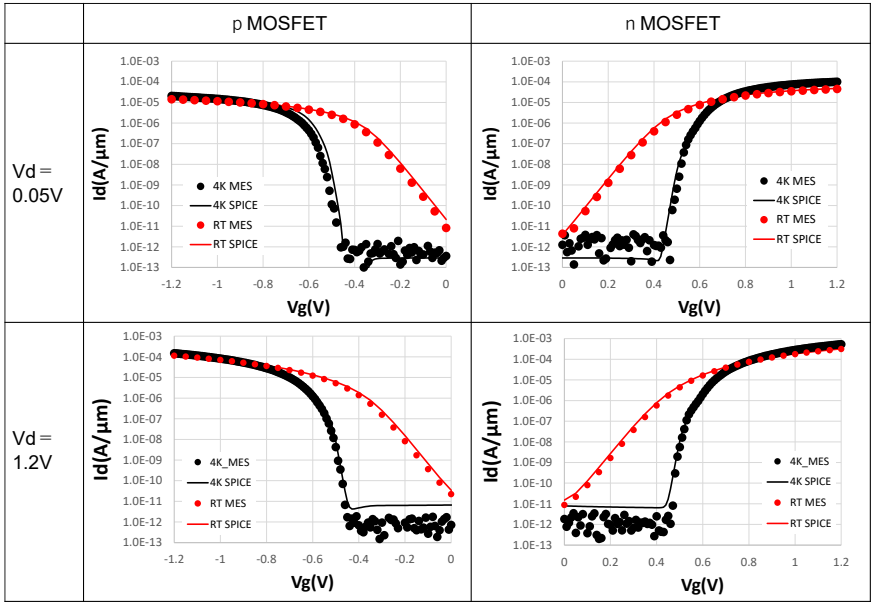
Development flow for a cell library



Flow of LSI design

Modelling of MOSFET

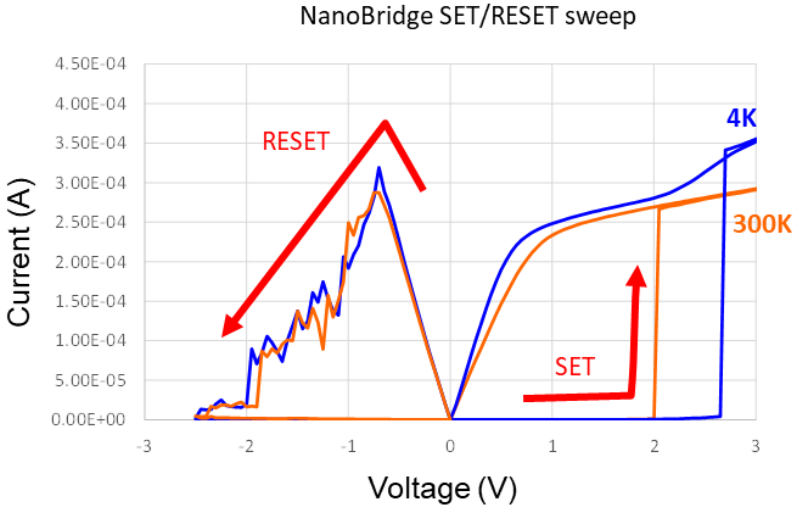
- As the temperature is decreased to 4K, we observe:
  - Steep subthreshold slope
  - Shift of threshold voltage
  - Increase of on-state current
  - Decrease of leakage current
- We fit the 4K data using RT models to reproduce the threshold voltage and the magnitude of on-state current.

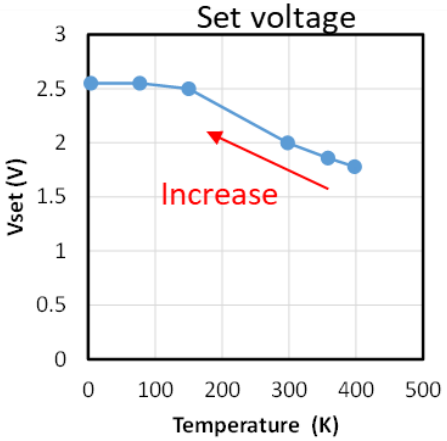


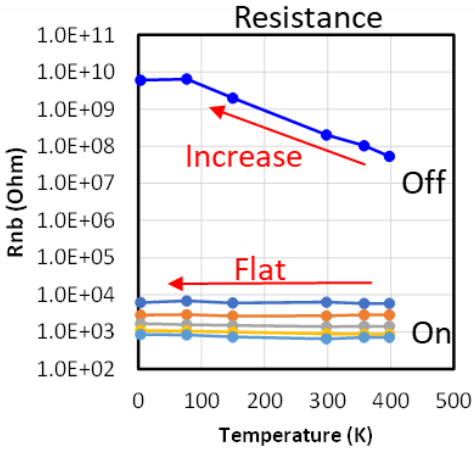
Tada, et al., IEEE Journal of Electron Device Society 2023

Temperature dependence of NanoBridge

- The programming voltage (V_{set}) of NanoBridge increases with decreasing T.
- R_{on} is independent of temperature, and R_{off} increases with decreasing temperature due to Poole–Frenkel emission mode.

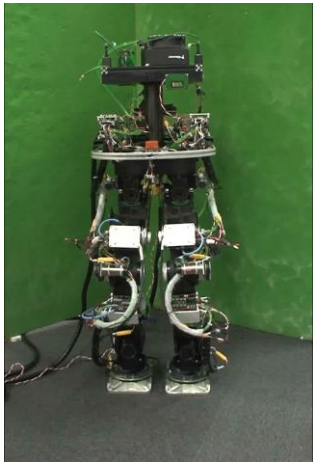


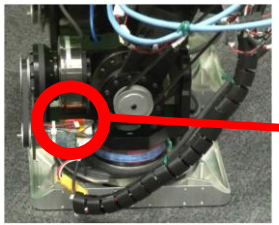




K. Okamoto et al., Jpn. J. Appl. Phys. **61**, SC1049 (2022).

Conclusions





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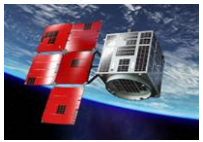
Tada, et al., IEEE IITC 2024



Acknowledgement

- This work is supported by New Energy and Industrial Technology Development Organization (NEDO). Project No. : JPNP16007.
- This work is supported by Japan Aerospace Exploration Agency (JAXA).
- The results have been achieved by “Research and development of innovative FPGA for satellite digitalization”, the Ministry of Education, Culture, Sports, Science and Technology (MEXT), JAPAN.
- This work is supported by Tsukuba Innovation Arena (TIA) and National Institute of Advanced Industrial Science and Technology (AIST).
- Thanks to NBS development and product department team.

Thank you

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1858

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