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Neuromorphic Electronics for Intelligence Everywhere

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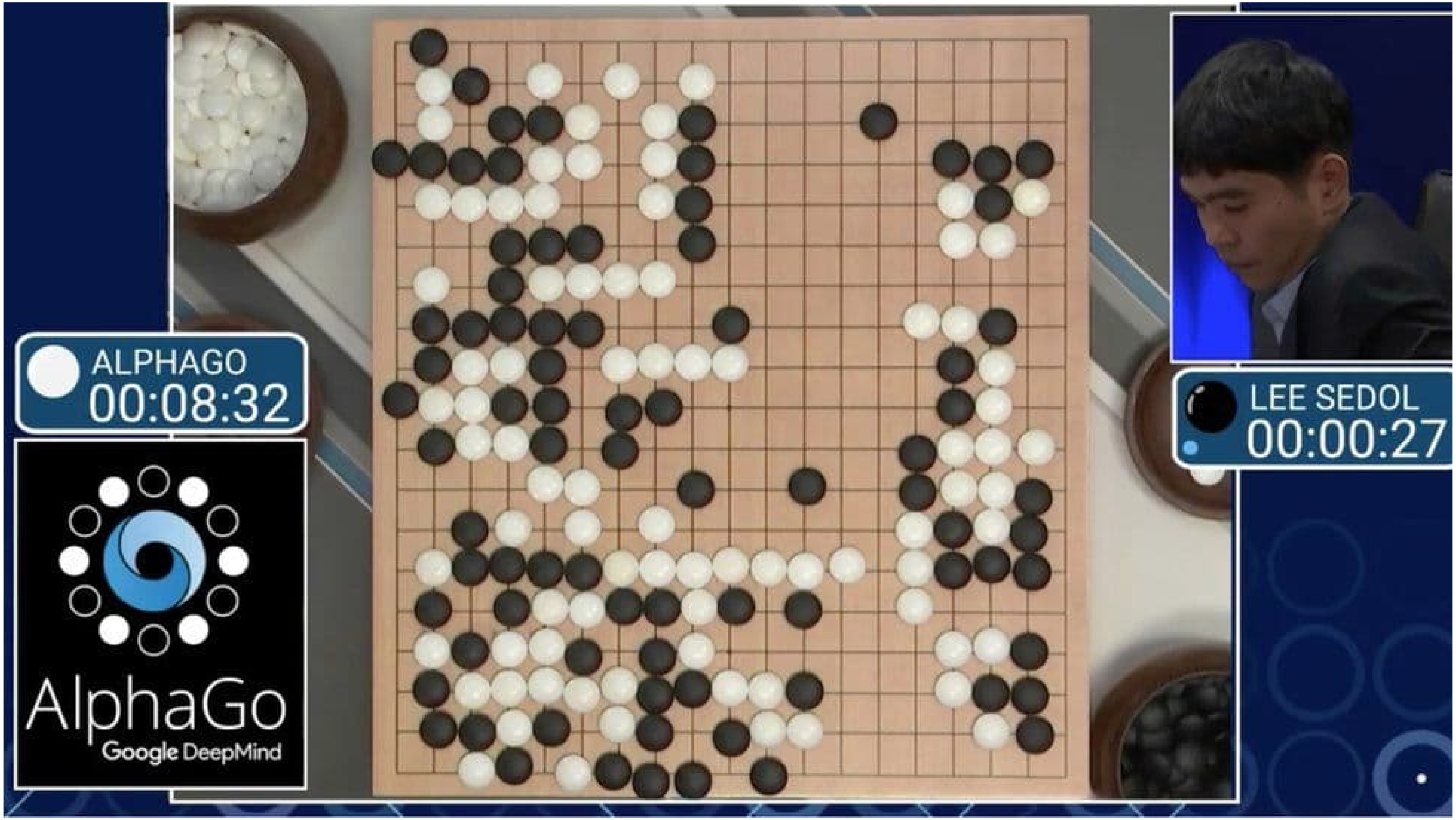
Advancement of AI



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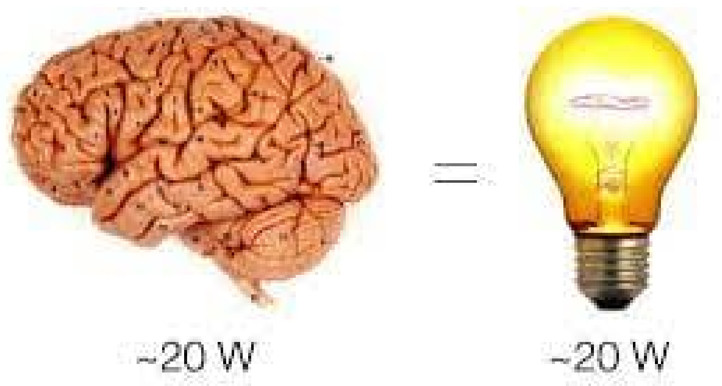
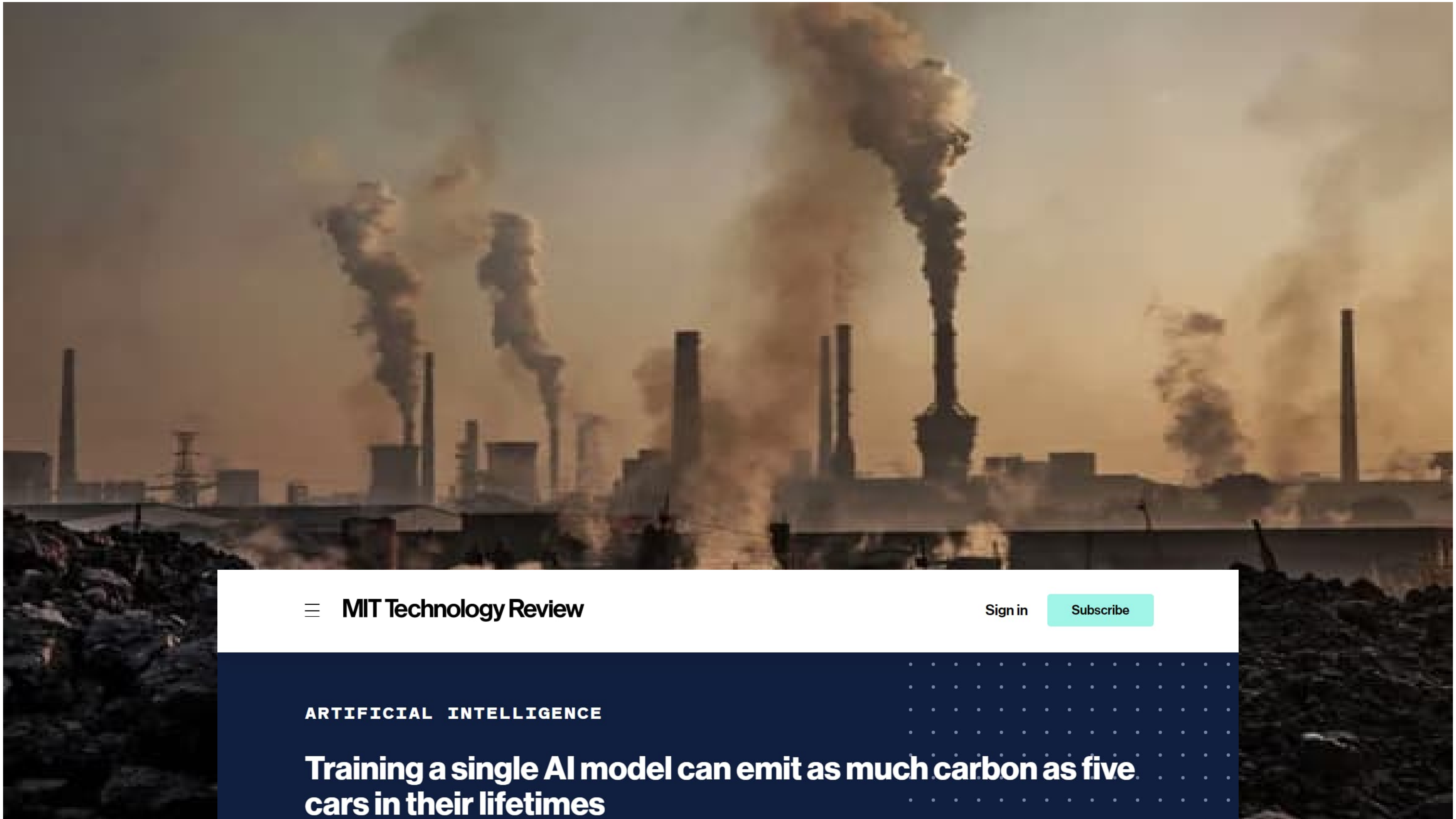
Cost of AI

Human brain



AI on HPC – Hundreds of MW



MIT Technology Review

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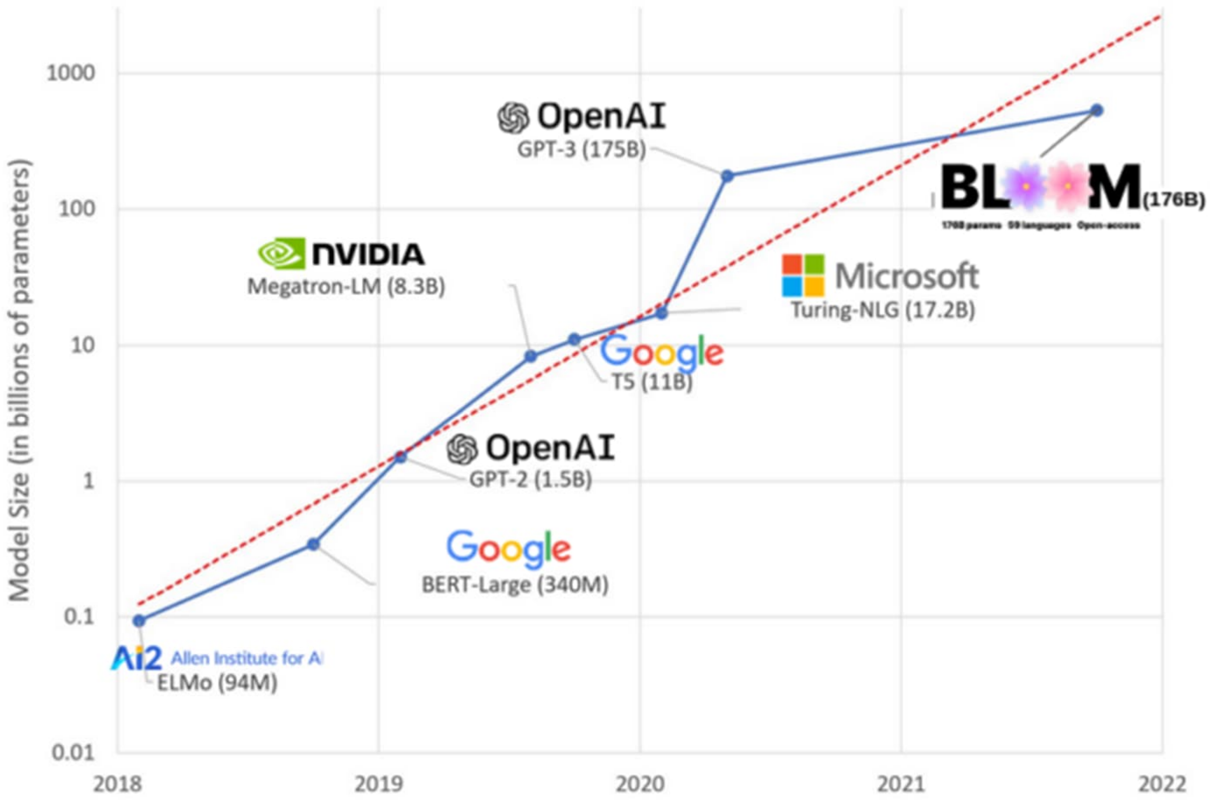
ARTIFICIAL INTELLIGENCE

Training a single AI model can emit as much carbon as five cars in their lifetimes

Deep learning has a terrible carbon footprint.

By Karen Hao

June 6, 2019



Model name	Number of parameters	Datacenter PUE	Carbon intensity of grid used	Power consumption	CO_2eq emissions	CO_2eq emissions × PUE
GPT-3	175B	1.1	429 gCO_2eq/kWh	1,287 MWh	*502 tonnes*	552 tonnes
Gopher	280B	1.08	330 gCO_2eq/kWh	*1,066 MWh*	*352 tonnes*	380 tonnes
OPT	175B	*1.09* [2]	*231 gCO_2eq/kWh*	*324 MWh*	70 tonnes	*76.3 tonnes* [3]
BLOOM	176B	1.2	57 gCO_2eq/kWh	433 MWh	25 tonnes	30 tonnes

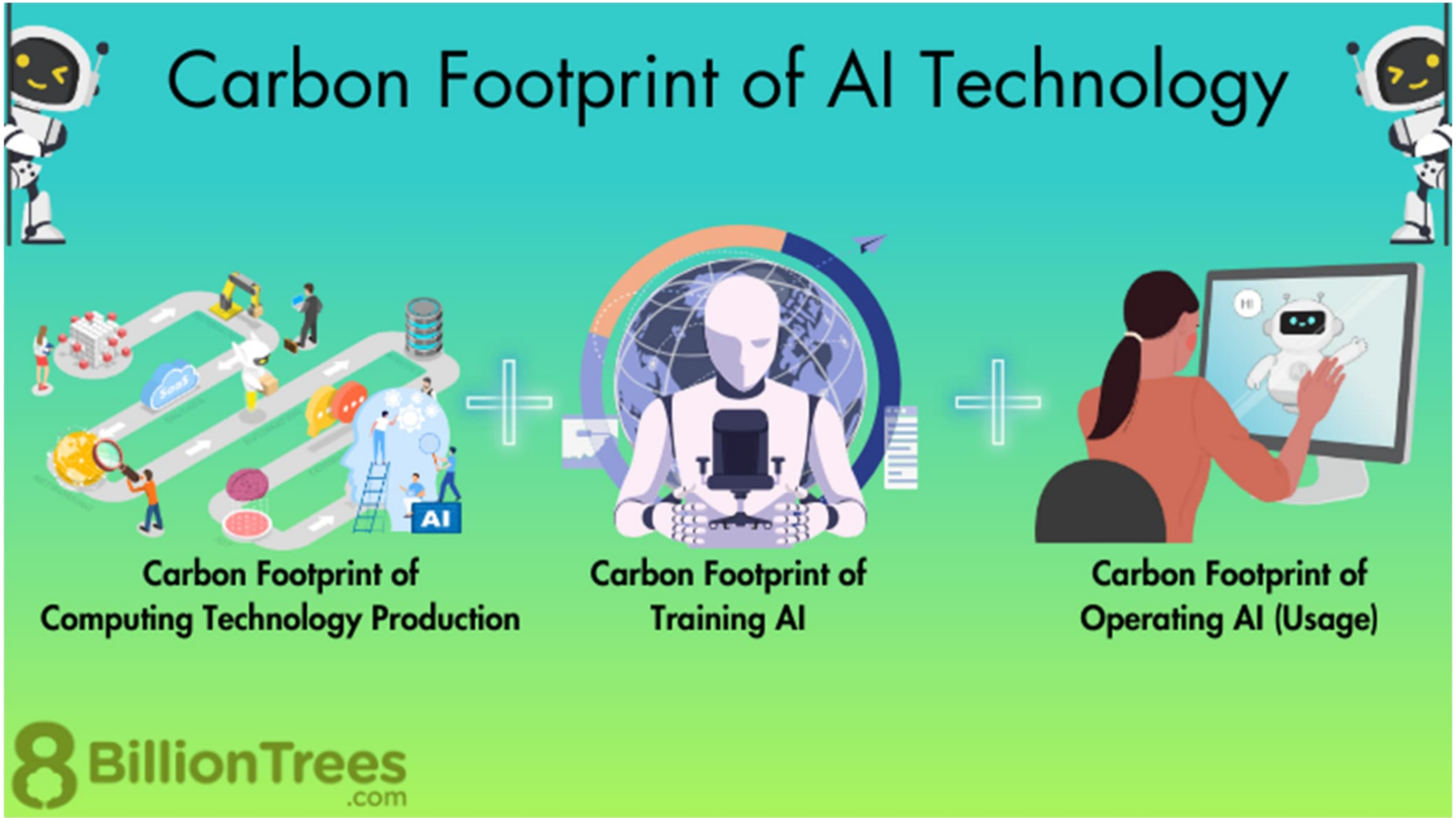
Table 4: Comparison of carbon emissions between BLOOM and similar LLMs. Numbers in *italics* have been inferred based on data provided in the papers describing the models.

https://arstechnica.com/gadgets/2023/04/generative-ai-is-cool-but-lets-not-forget-its-human-and-environmental-costs/

Data centres will use twice as much energy by 2030 — driven by AI

Upgrades to electricity grids might not keep up with the demands of power-hungry data centres. Nature.com: *doi: https://doi.org/10.1038/d41586-025-01113-z*

AI carbon footprint

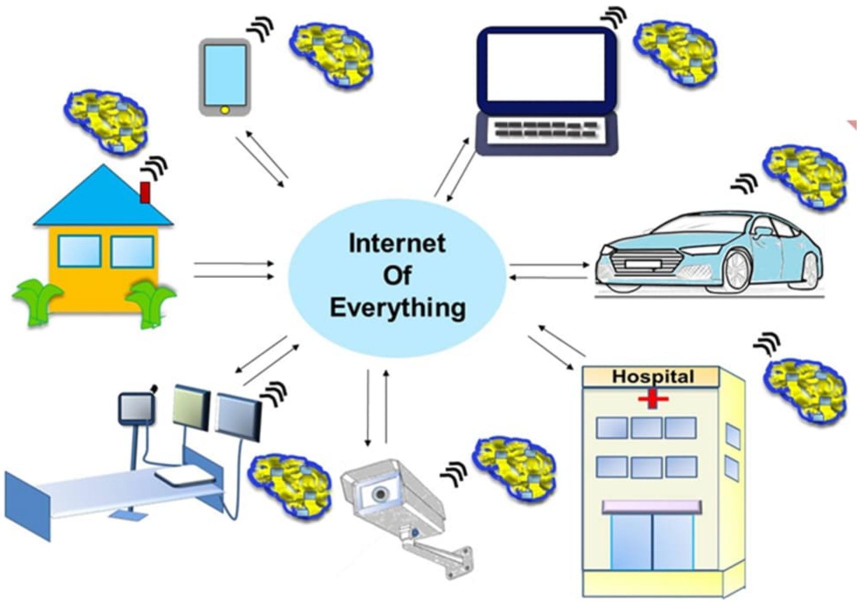


Solution

- Take inspiration from nature
- Memory-centric Computing
- Adding computation to sensory nodes

Edge Intelligence Needs

a



Digitize All data

Sensor → ADC → Digital Processor

With Analog data processing

Sensor → Analog Processor → ADC → Digital Processor

Less data communication

Faster, Energy-efficient, Secure

Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 4, 2100175 (2022).

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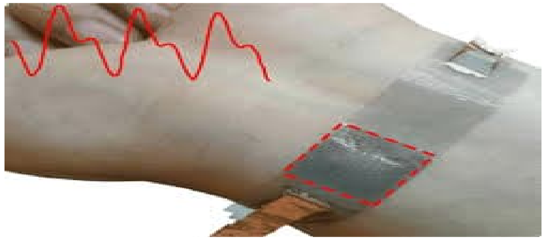
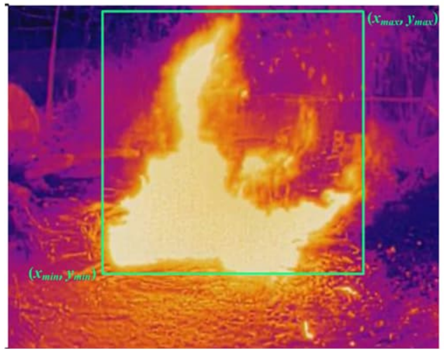
Applications

Wearable health monitor



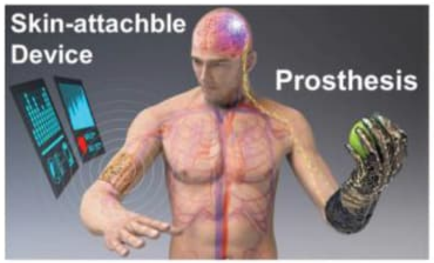
Security & Surveillance

Environmental monitor

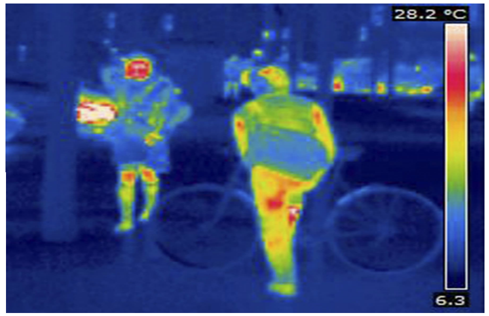


Early detection
of fire hazards

Sensing



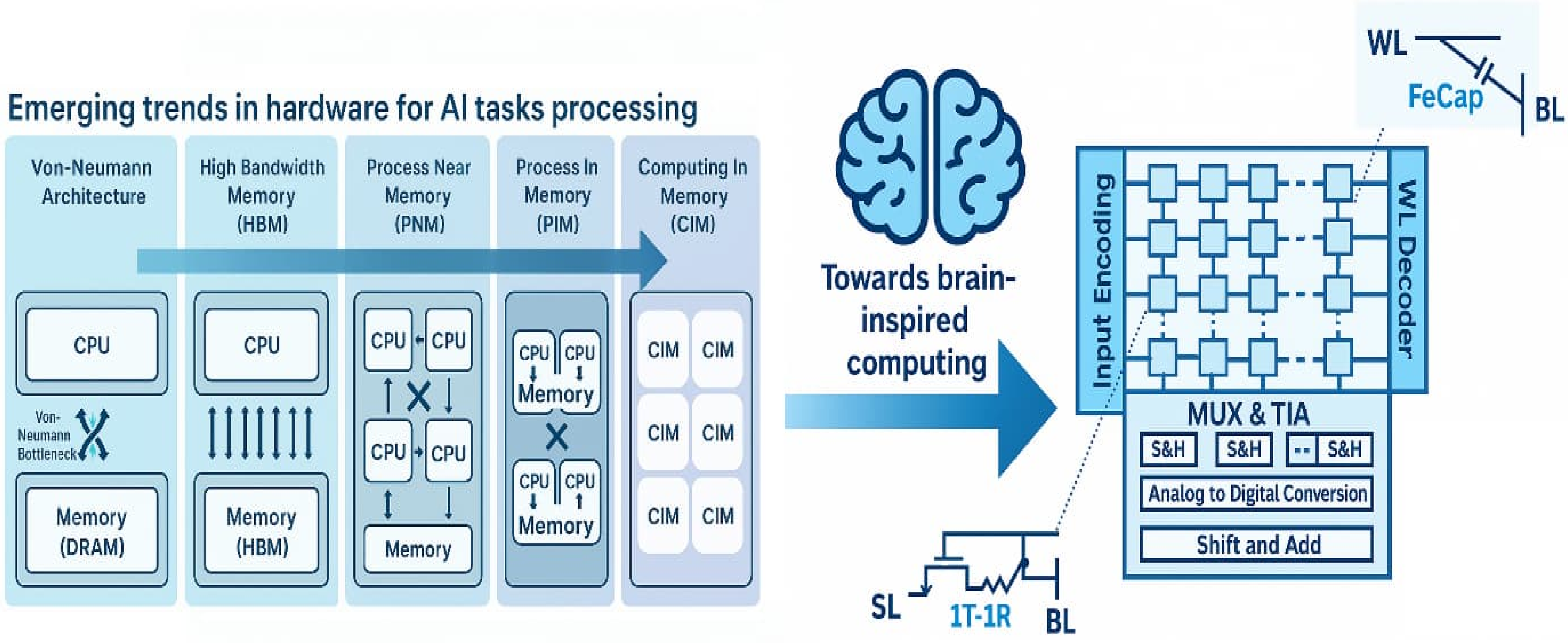
Prosthetics Robotics



Traffic safety in dark

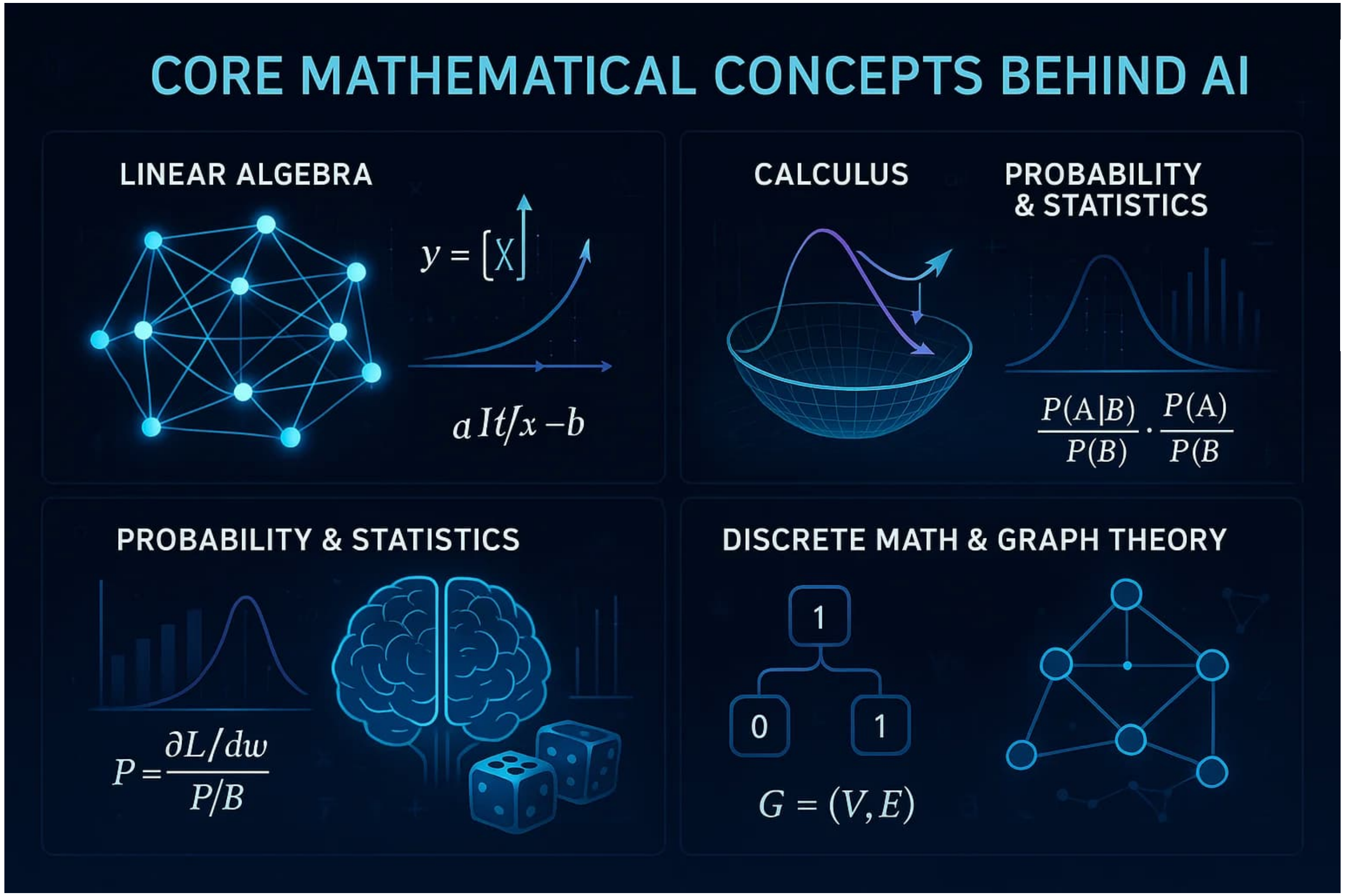
Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 4, 2100175 (2022).

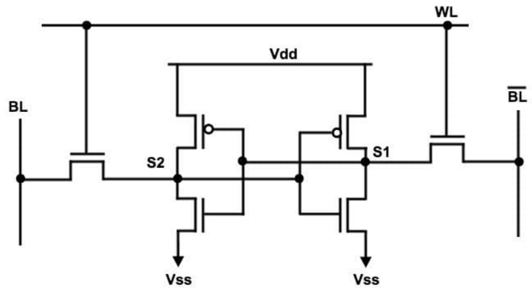
Hardware Evolution for AI

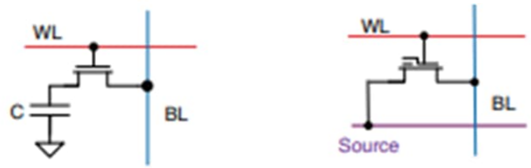


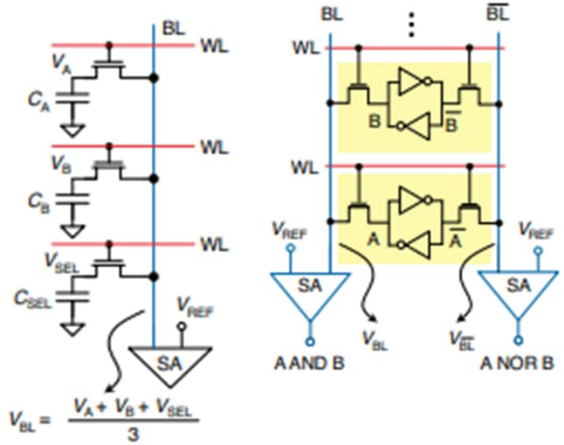
Towards Capacitive In-Memory-Computing: A Device to Systems Level Perspective on the Future of AI Hardware
Kapil Bhardwaj, Ella Paasio and Sayani Majumdar, 2025, Adv. Intell. Discov. https://arxiv.org/abs/2508.13225

Current AI HW – Replicating Mathematical fuctions with traditional components

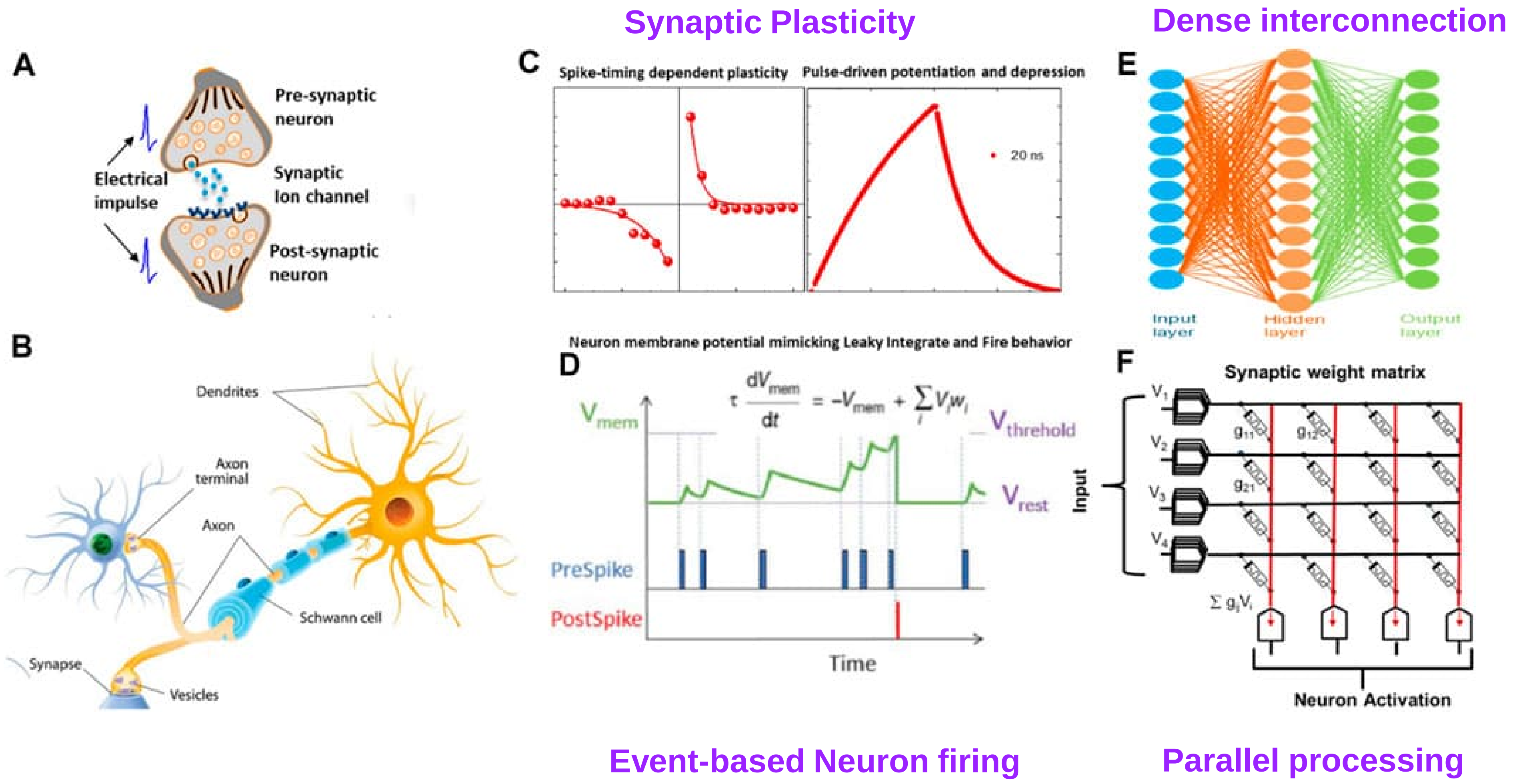








Future AI HW – Replicating Biological Brain with Device Physics



Harnessing ferroic ordering in thin film devices for analog memory and neuromorphic computing applications down to deep cryogenic temperatures, Sayani Majumdar, Front. Nanotechnol., 2024, Sec. Nanoelectronics, Volume 6 | https://doi.org/10.3389/fnano.2024.1371386

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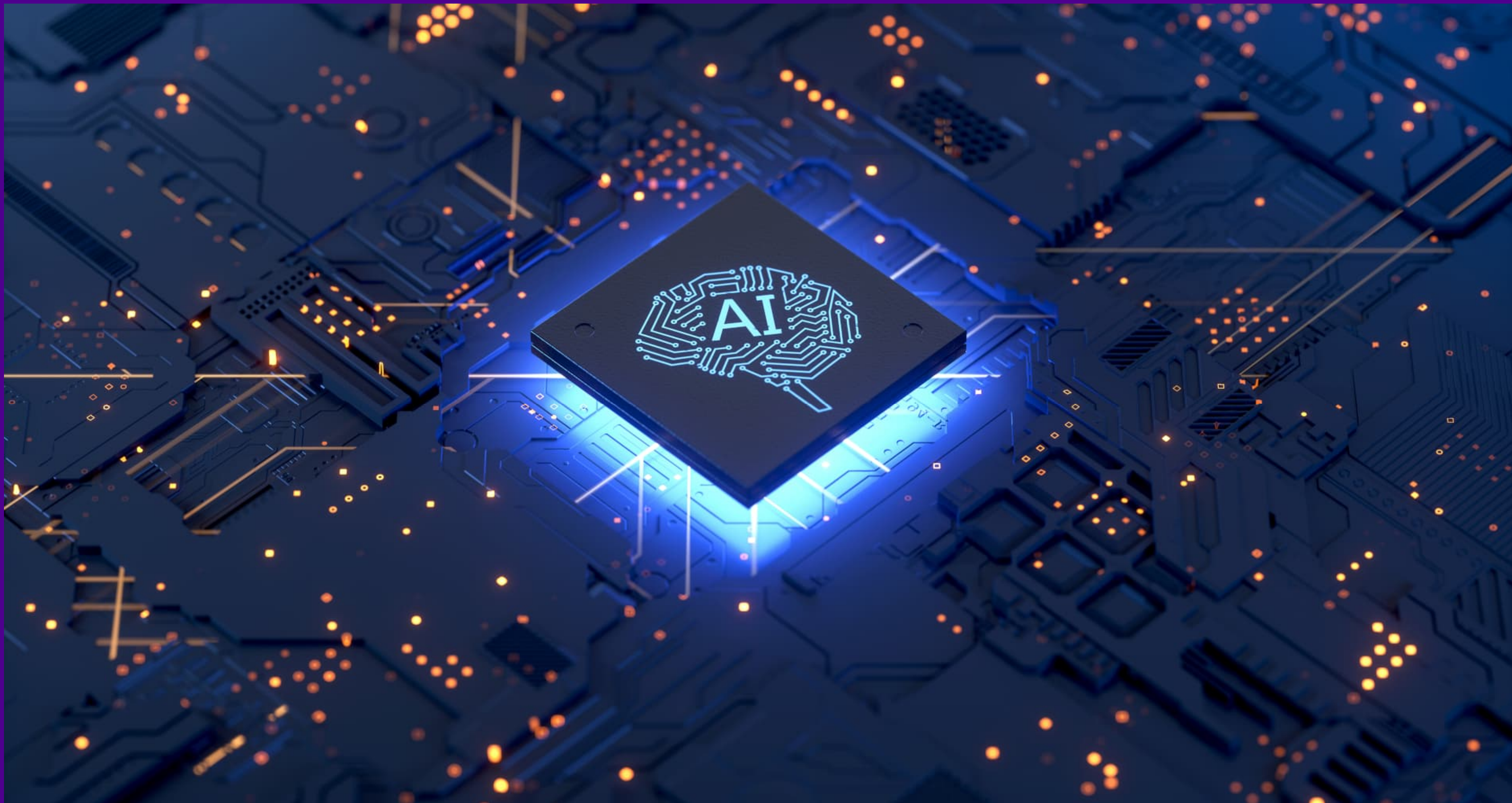
Neuromorphic Research in Europe



Key European Neuromorphic Initiatives and Projects

- EBRAINS & Human Brain Project (HBP): EBRAINS, a digital research infrastructure derived from the HBP, supports two major, complementary large-scale neuromorphic machines:
  - SpiNNaker (Manchester, UK): A massively parallel system connecting 1 million ARM processors.
  - BrainScaleS (Heidelberg, Germany): A physical model machine using analog electronics to simulate neurons.
- NeurotechEU: A European University Alliance dedicated to neurotechnology.
- NEUROTEC & JUNCA (Germany): A collaboration between Forschungszentrum Jülich and RWTH Aachen to develop neuro-inspired AI hardware.
- EU Horizon Projects:
  - NeurONN: Develops two-dimensional Oscillatory Neural Networks for low-power AI.
  - PlasmoniAC: Focuses on plasmonic-based neuromorphic chips for ultra-high energy efficiency.
  - NEUROPULS & Quromorphic: Exploring photonic (light-based) and quantum-level neuromorphic computing.
  - TEMPO: Advanced 3D interconnection technologies and emerging memory devices (OxRAM, FeRAM).
  - NimbleAI: Focuses on neuromorphic sensing and processing for edge applications.

Key Research Areas and Technologies

Memristive Technology: Memristors for replicating synaptic functions (storage and processing), Leaky-integrate-and-fire (LIF) Neurons and non-volatile memory.

Spiking Neural Networks (SNNs): Research is centered on developing SNN algorithms that are more efficient at processing temporal data than standard Deep Neural Networks (DNNs).

Materials Science: Researching novel materials for neuromorphic devices, such as ferroelectric field-effect transistors (FeFETs) at Fraunhofer IPMS and 2D materials for optical neurons (2DFERROPLEX).

Edge Computing & Sensory Processing: Developing chips that combine sensing and computing, such as the **NeuroPsense** project (event-based vision)

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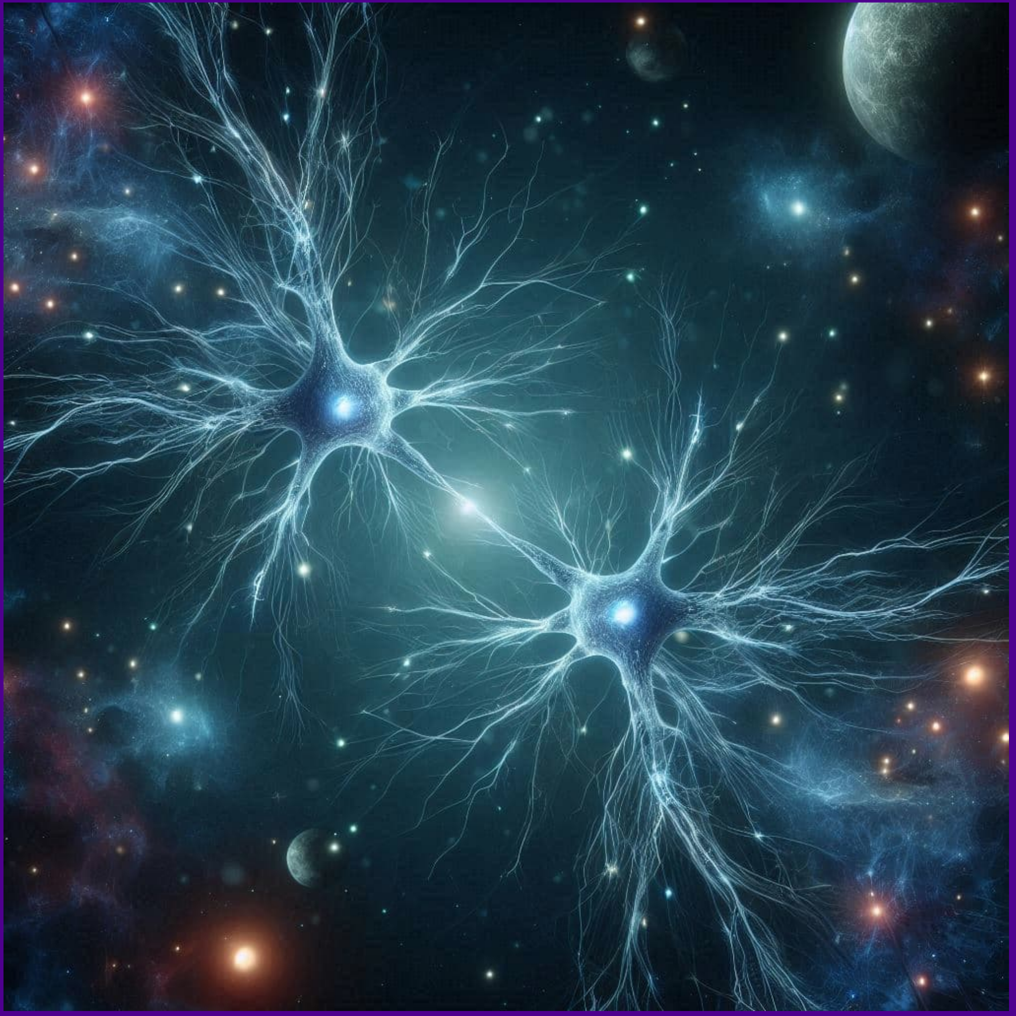
European Neuromorphic Research Day

INL INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY

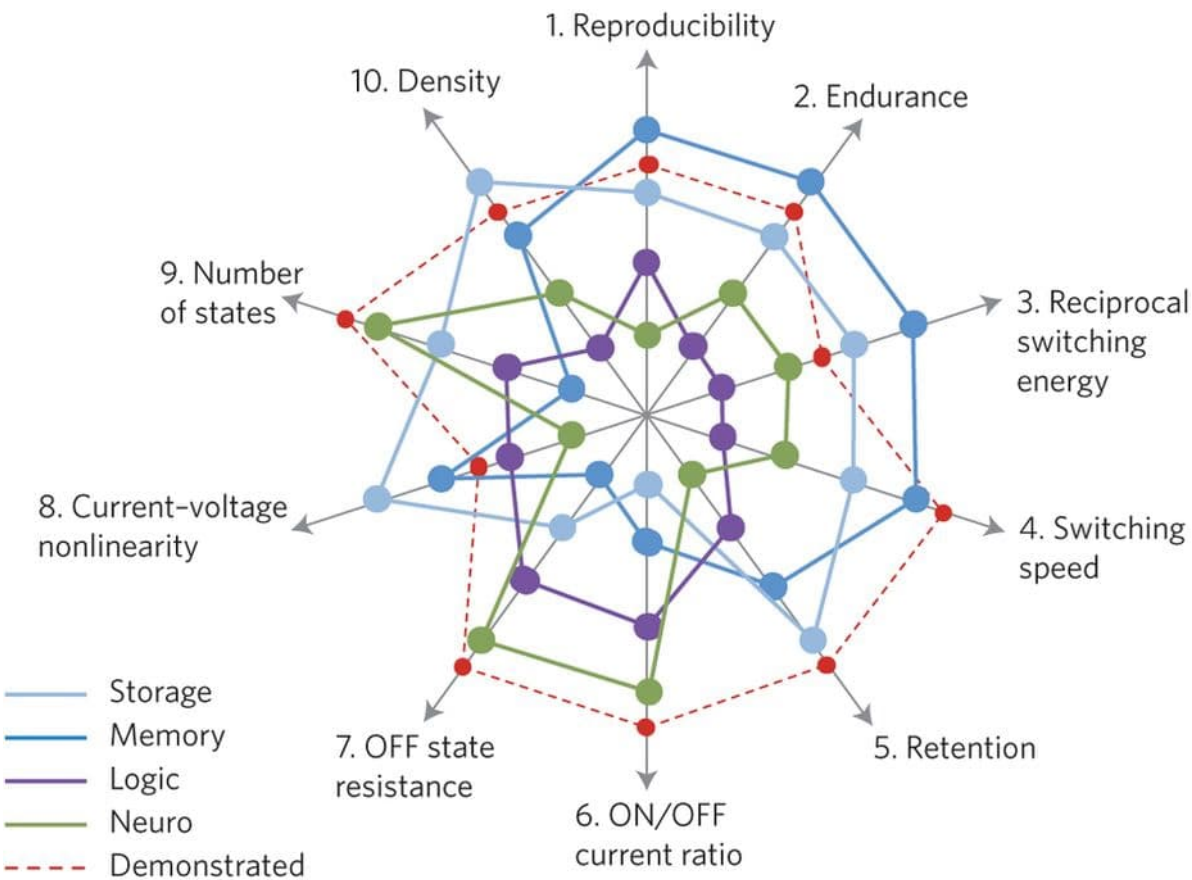
RESEARCH INNOVATION SERVICES CAREERS SOCIETY ABOUT

European Neuromorphic Computing Event Draws 100 Participants to Bridge Research and Innovation

Hardware for Brain-Inspired Computing



In-Memory Computing Needs from Memory Devices



Additionally:

- Scalability
- CMOS compatibility
- Fault tolerance
- Noise insensitivity
- Compatibility with other materials on-chip
- Temperature window

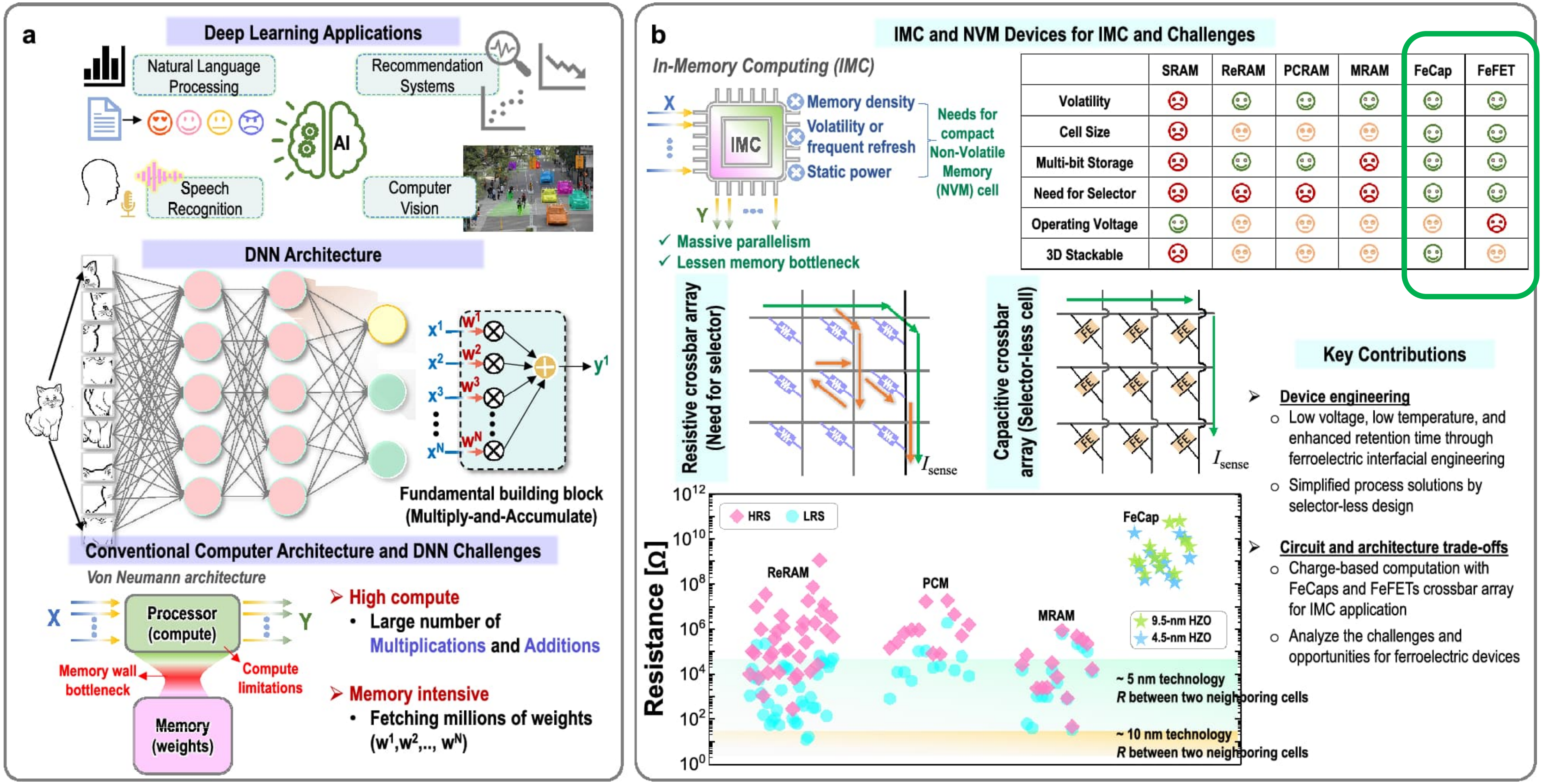
Memristive devices for computing. J. J. Yang, D. B. Strukov, D. R. Stewart. Nat. Nanotech. 8, 13 – 24 (2013)

Current Memory Landscape

Performance indices	CMOS memories		Emerging memristive memories						
	NOR Flash	NAND Flash	RRAM	PCM	STT-MRAM	FeRAM	FeFET	SOT-MRAM	Li-ion
On/off ratio	10^4	10^4	10^2	10^4	2	10^3	10^4	2	10^3
Multilevel operation	2-bit	4-bit	2-bit	2-bit	1-bit	1-bit	5-bit	1-bit	10-bit
Write voltage	<10 V	>10 V	<3 V	<3 V	<1.5 V	<3 V	<5 V	<1.5 V	<1 V
Write energy (/bit)	100 pJ	10 fJ	0.1–1 pJ	10 pJ	100 fJ	100 fJ	<1 fJ	<100 fJ	100 fJ
Write time	1–10 µs	0.1–1 ms	<10 ns	<10 ns	<10 ns	30 ns	10 ns	<10 ns	<10 ns
Read time	50 ns	10 µs	<10 ns	<10 ns	<10 ns	<10 ns	<10 ns	<10 ns	<10 ns
Endurance	10^5	10^4	10^5–10^8	10^6–10^9	10^{15}	10^{10}	10^{11}	10^{15}	$>10^5$
Retention	Long	Long	Medium	Long	Medium	Long	Long	Medium	–
Drift	No	No	Weak	Yes	No	No	No	No	No
Linearity	Low	Low	Low	Low	None	None	Low	None	High
Integration density	High	Very high	High	High	High	Low	High	High	Low
Suitability for DNN training	No	No	No	No	No	No	Moderate	No	Yes
Suitability for DNN inference	Yes	Yes	Moderate	Yes	No	No	Yes	No	Yes
Suitability for SNN applications	Yes	No	Yes	Yes	Moderate	Yes	Yes	Moderate	Moderate

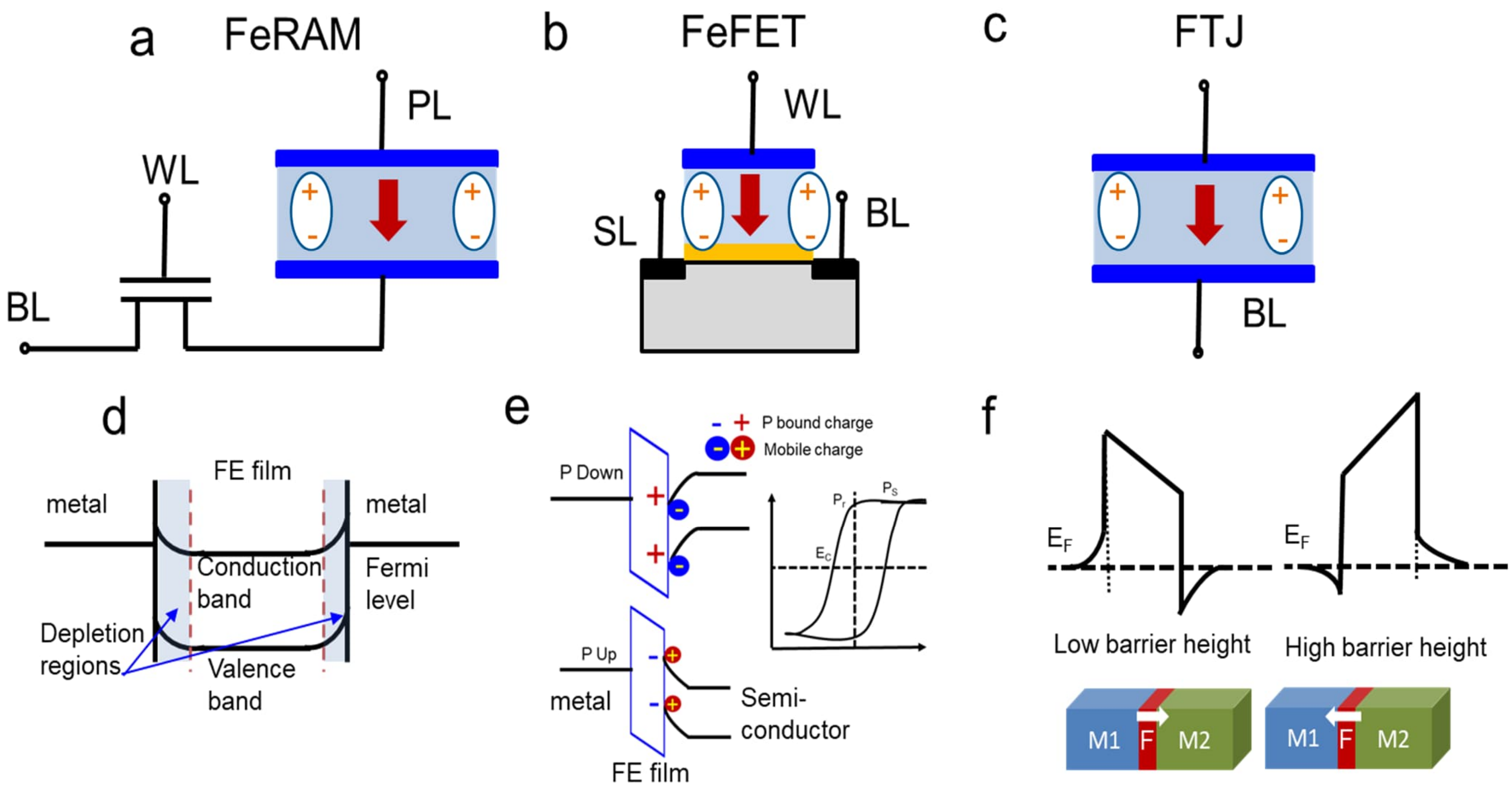
Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 4, 2100175 (2022).

IMC with Ferroelectric Devices



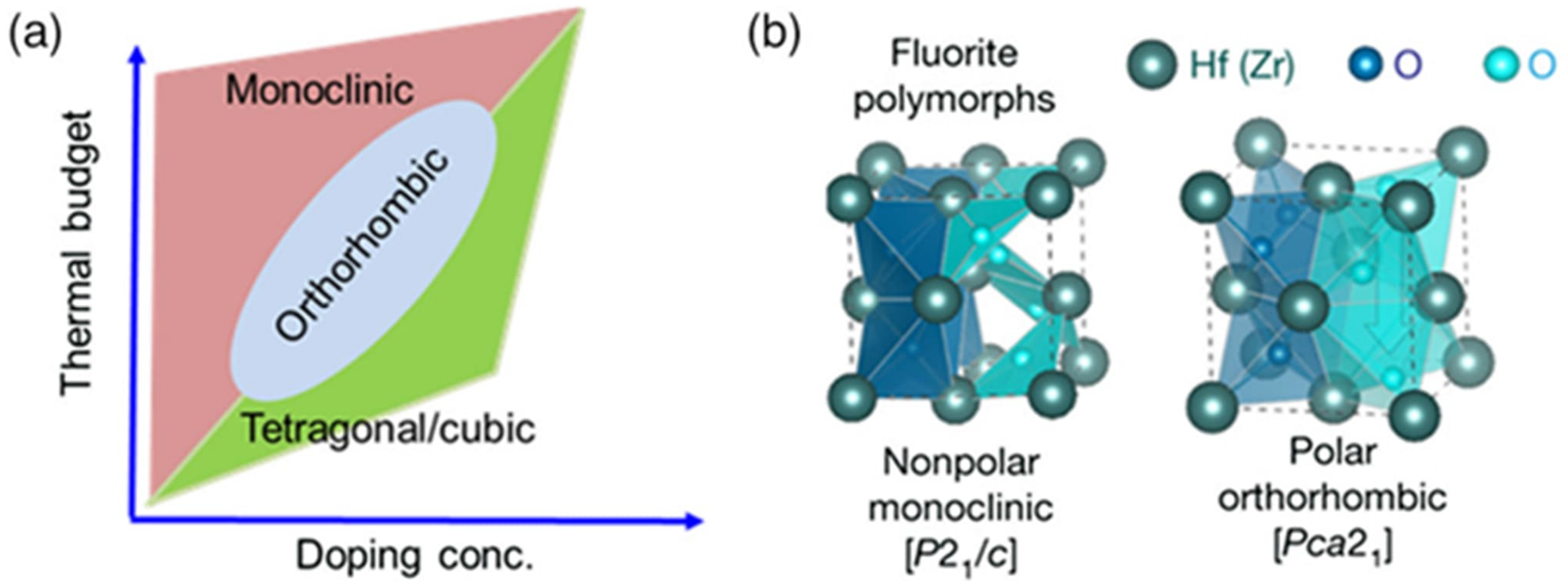
Ferroelectric capacitors and field-effect transistors as in-memory computing elements for machine learning workloads, Scientific Reports volume 14, Article number: 9426 (2024)

Ferroelectric memories



Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 4, 2100175 (2022).

CMOS Back-end compatible Ferroelectric – Hf-Zr-O_2



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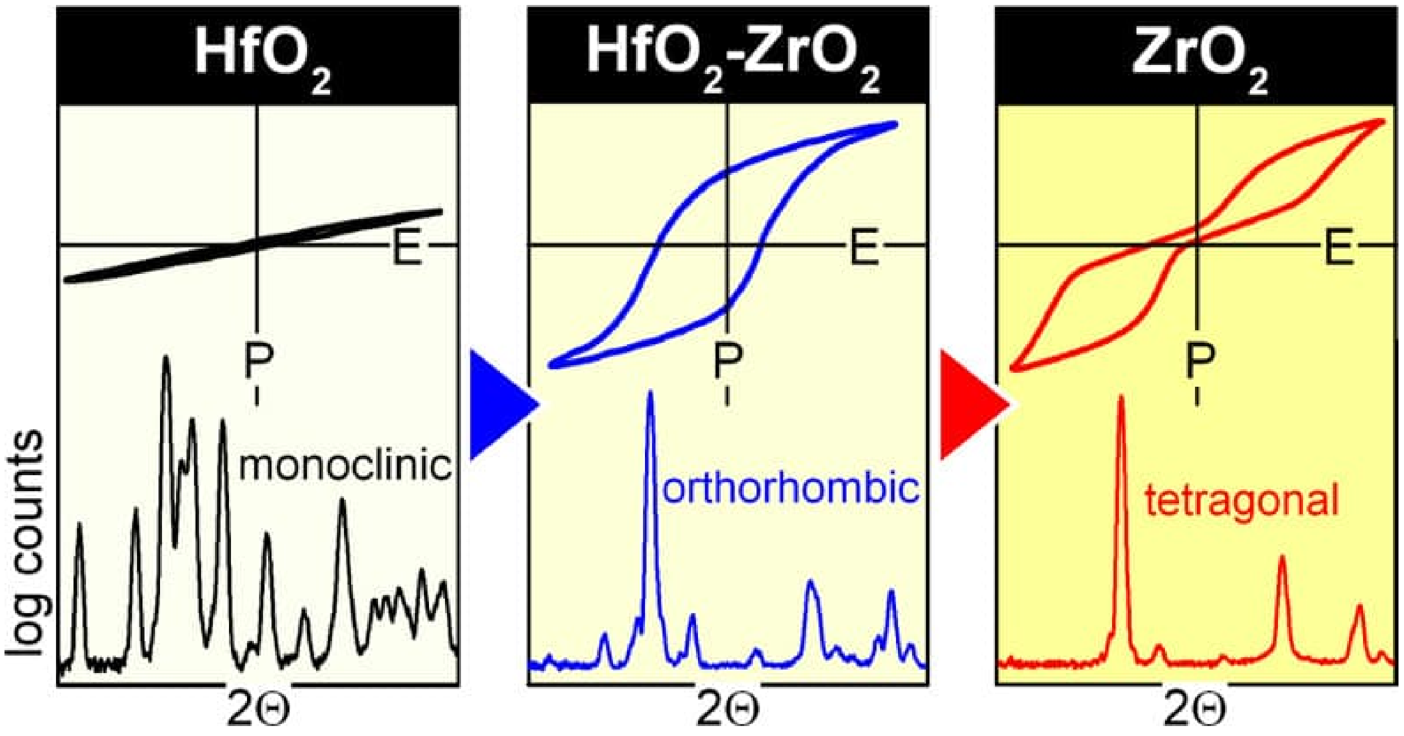
CMOS Back-end compatible Ferroelectric

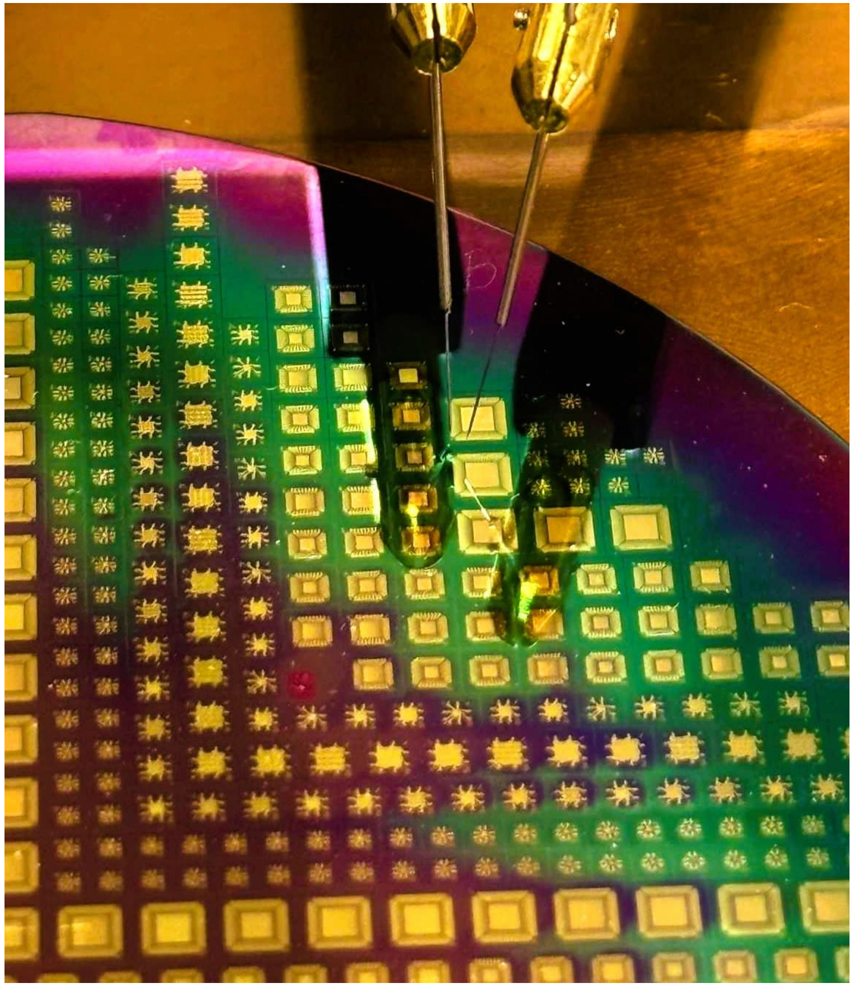


Nano Lett. 2012, 12, 8, 4318–4323

Fabrication – CMOS, Beyond CMOS and Hybrid

Process complexity and cost considerations

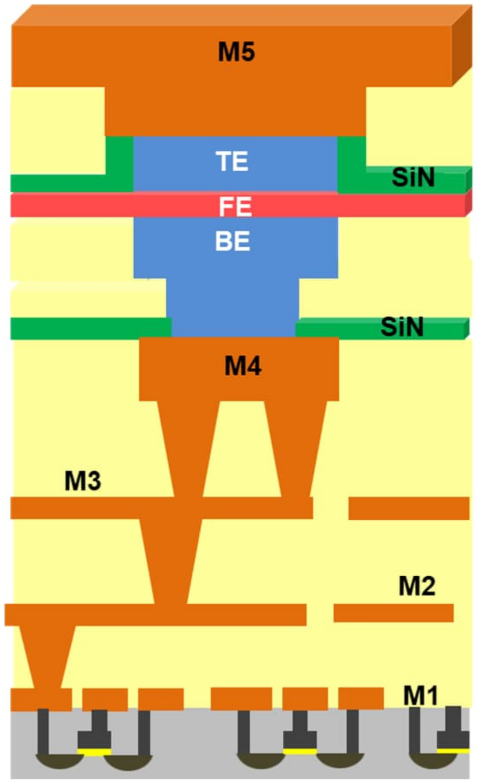
1. Dense integration possibilities – footprint, 3D stackability
2. Process complexity and standard fab compatibility
3. Logic compatibility
4. Thermal effects



Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 4, 2100175 (2022).

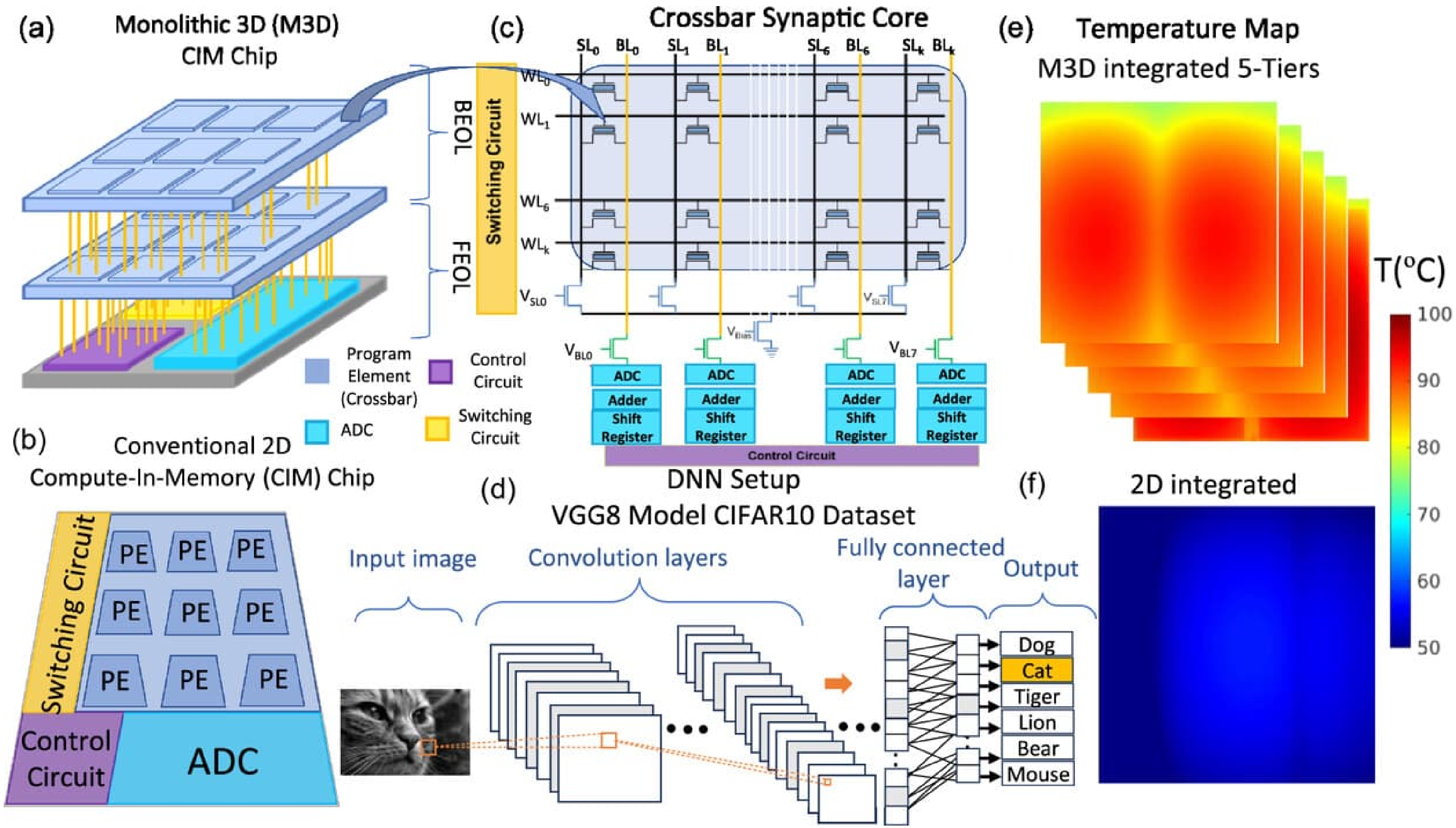
CMOS Compatibility

- Monolithic integration requires material and process compatibility with CMOS
- Continuous downscaling of CMOS transistors pushing **the driving voltage limit to <1.5V**.
- **Maintaining distinguishable multiple programmable states** within this limit is the biggest challenge.
- Also **process compatibility of sensor and memory** components is a critical issue.



Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 2100175 (2021).

Thermal effects of 3D BEoL integrated Chips



Thermal Effects on Monolithic 3D Ferroelectric Transistors for Deep Neural Networks Performance, S. Kumar et al, Advanced Intelligent Systems, 6, 2024, 2400019

CMOS and beyond: Devices and Systems Research Group

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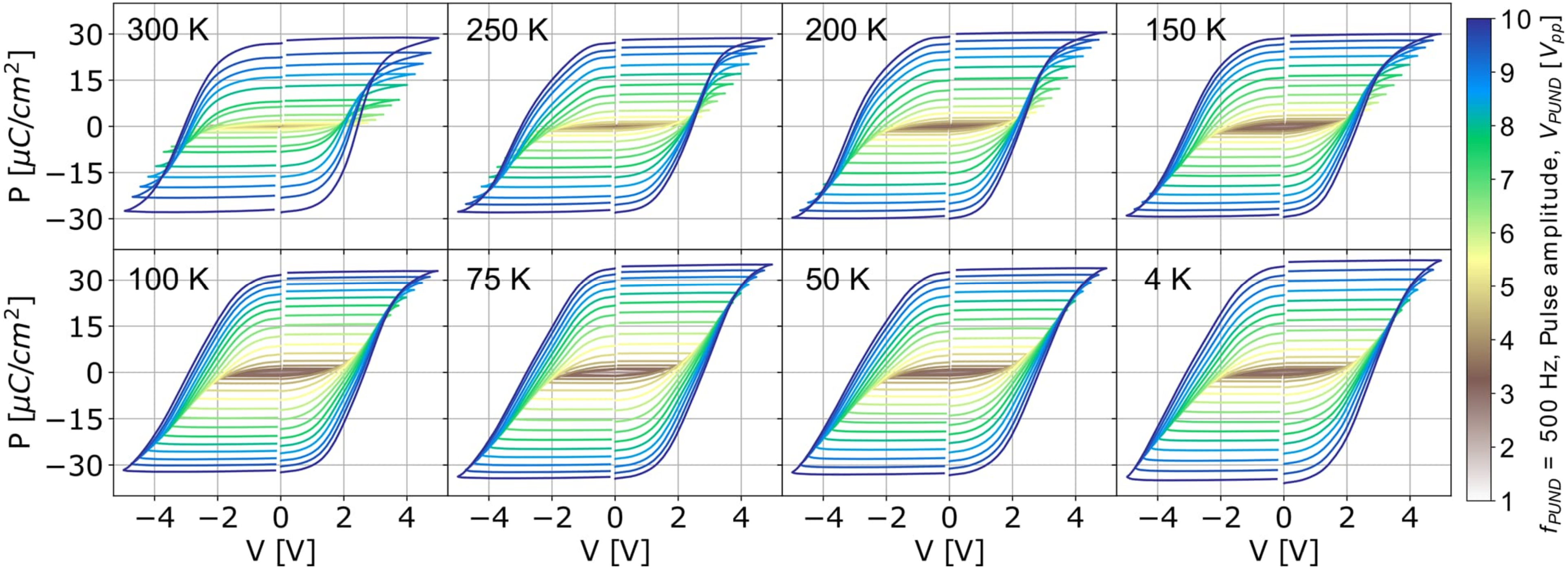
CMOS and Beyond: Devices and Systems Research Group

CMOS and Beyond group at the Faculty of Information Technology and Communication Sciences of Tampere University focuses on research of Advanced Semiconductor Devices and Systems for next generation of Computing like Neuromorphic and Quantum Computing.

Research | Teaching

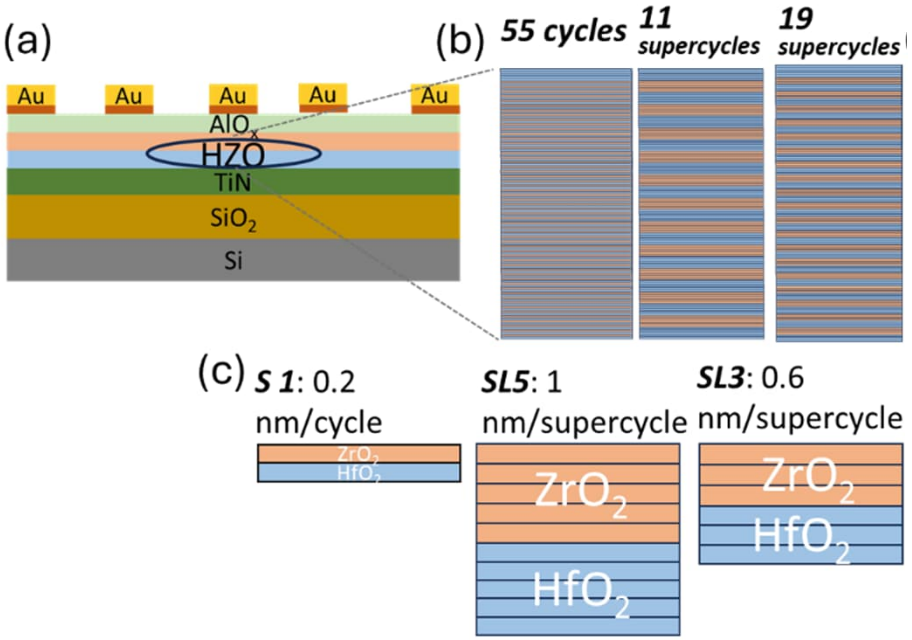
https://research.tuni.fi/cmos-and-beyond/

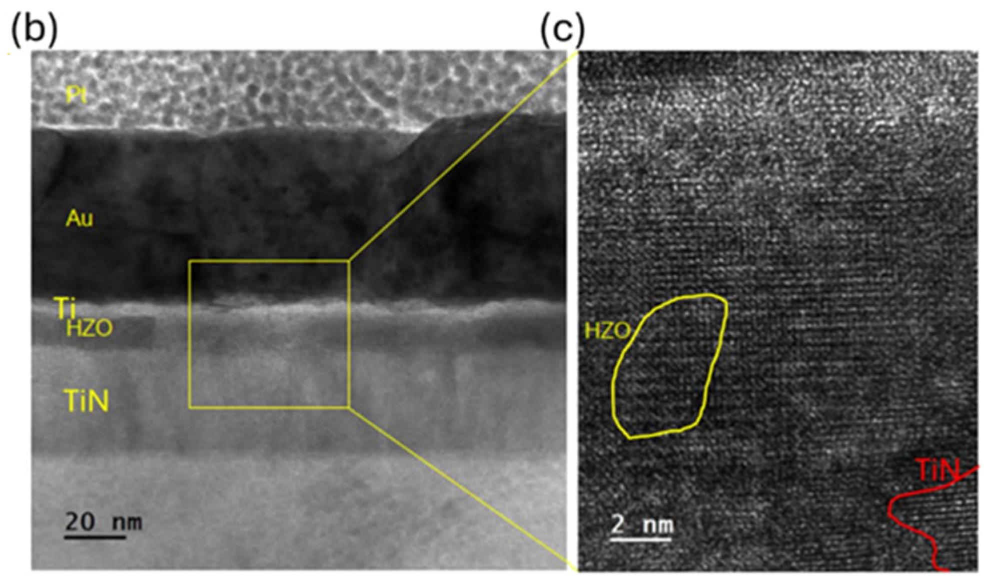
HZO FeCAPs – Operation down to cryo-temperatures



Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for Analog Memory and In-Memory Computing Applications down to Deep Cryogenic Temperatures, H Bohuslavskyi, K Grigoras, M Ribeiro, M Prunnila, S Majumdar, Adv. Electron. Mater. 10 (7), 2300879 (2024).

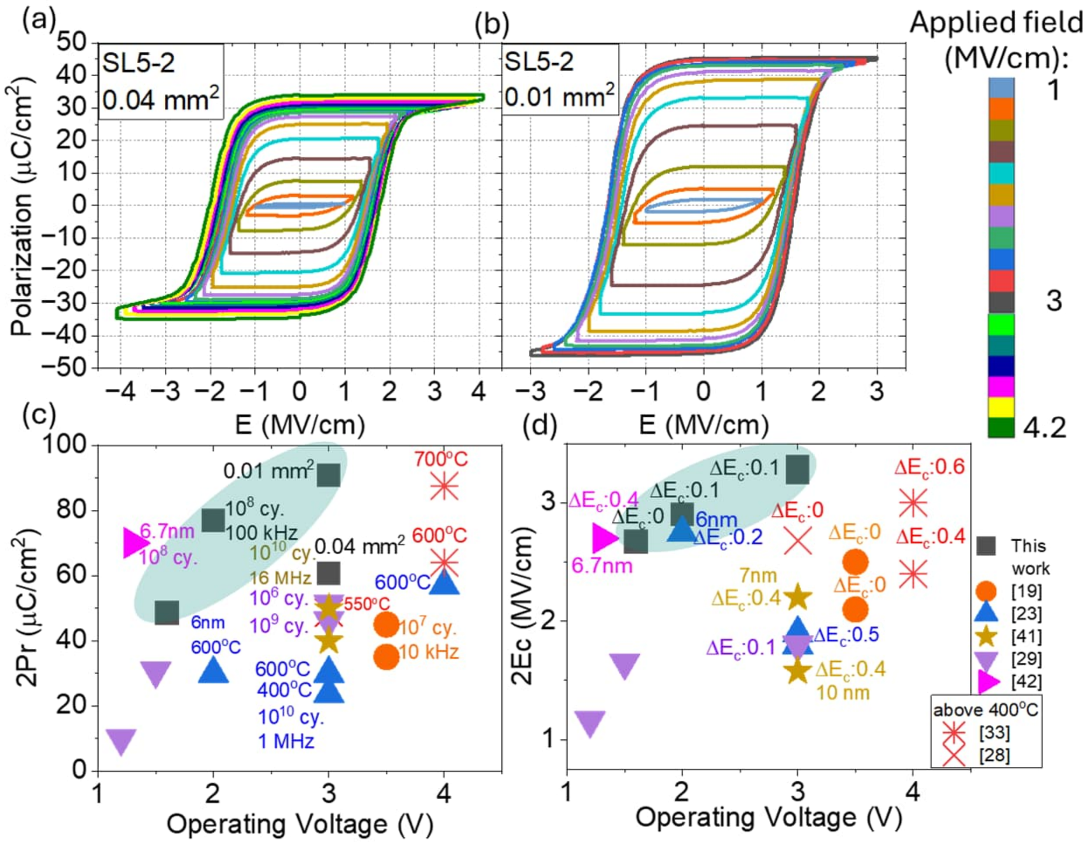
Low Voltage Ferroelectric Capacitor – Highest $2P_r$ at 2V





Record High Polarization at 2V and Imprint-free operation in Superlattice HfO2-ZrO2 by Proper Tuning of Ferro and Antiferroelectricity; X. Li, P. Srivari, S Majumdar et al.; Adv. Mater. Tech. e02027, 2026 https://arxiv.org/abs/2509.07045

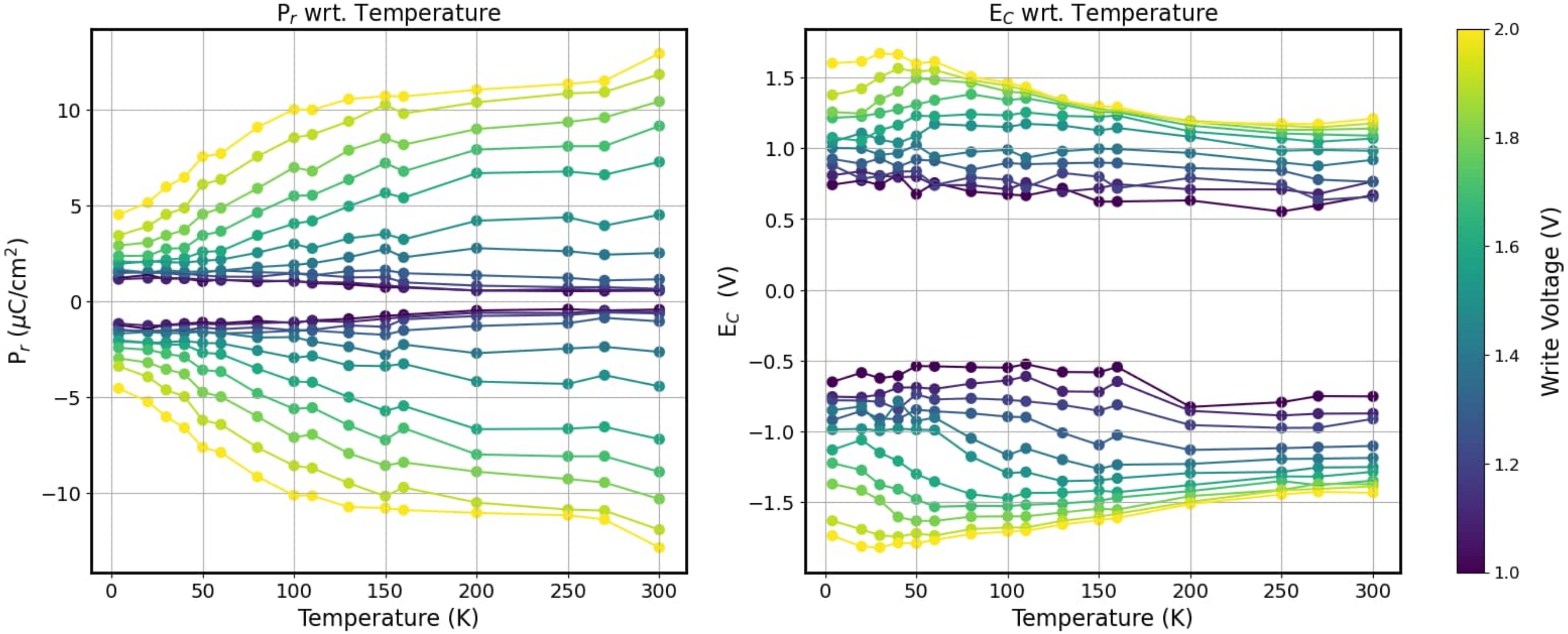
Low Voltage Ferroelectric Capacitor – Highest $2P_r$ at 2V



DOI : 10.1002/admt.202502027

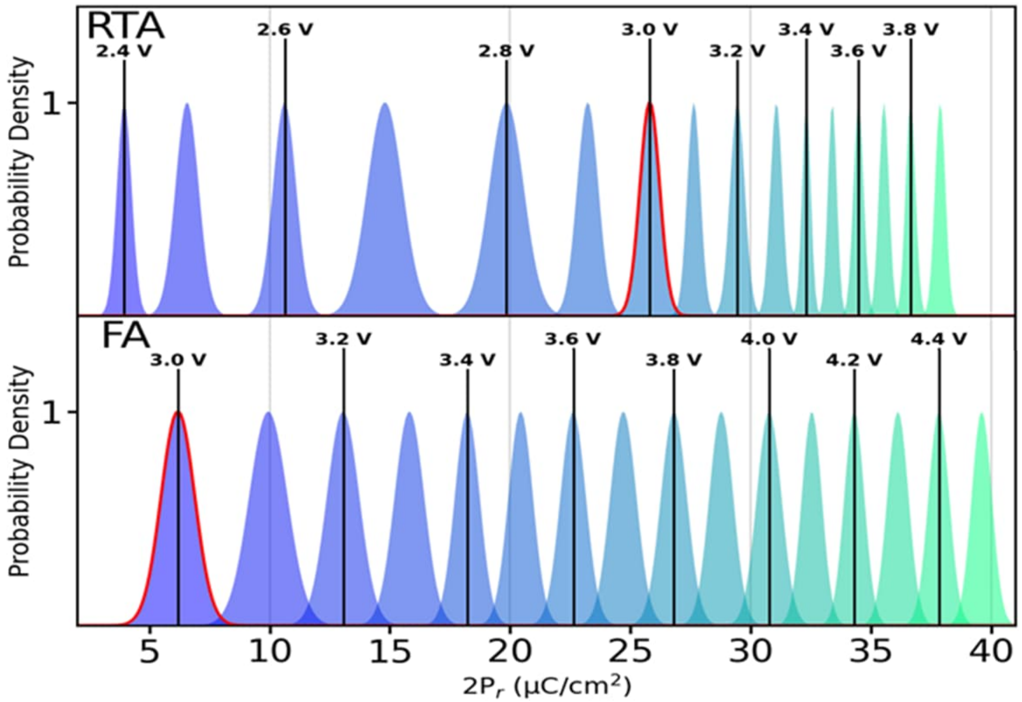
Record High Polarization at 2V and Imprint-free operation in Superlattice HfO2-ZrO2 by Proper Tuning of Ferro and Antiferroelectricity; X. Li, P. Srivari, S Majumdar et al.; Adv. Mater. Tech. e02027, 2026 https://arxiv.org/abs/2509.07045

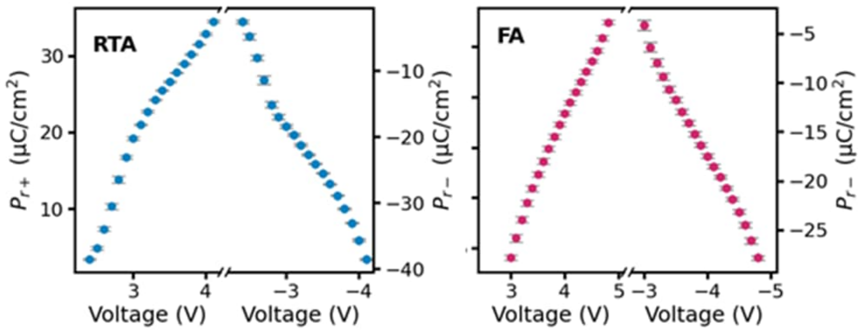
FeCap – Low voltage Cryogenic operation down to 4K

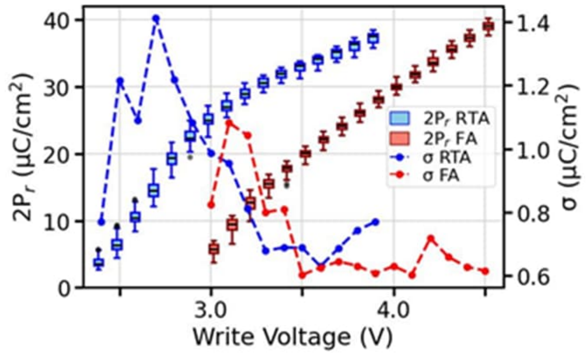


R. Ranta, E. Paasio, S. Majumdar (Manuscript in preparation).
Master's thesis, Rikhard Ranta: https://aaltodoc.aalto.fi/server/api/core/bitstreams/1167b1f1-b175-4daf-9051-c0e6d8f37e89/content

Analog State Reliability – Samples annealed at 450 & 350 ˚C

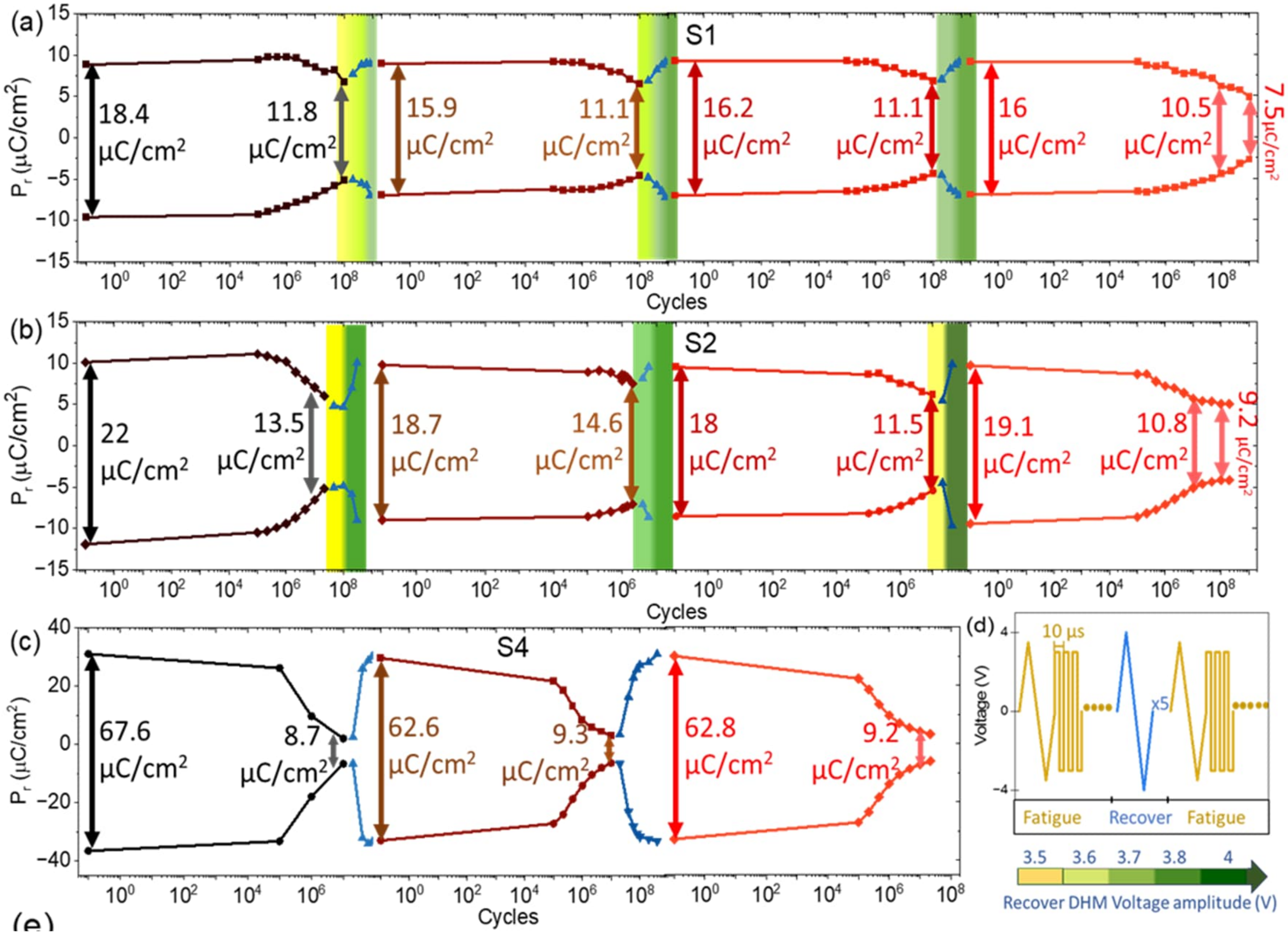






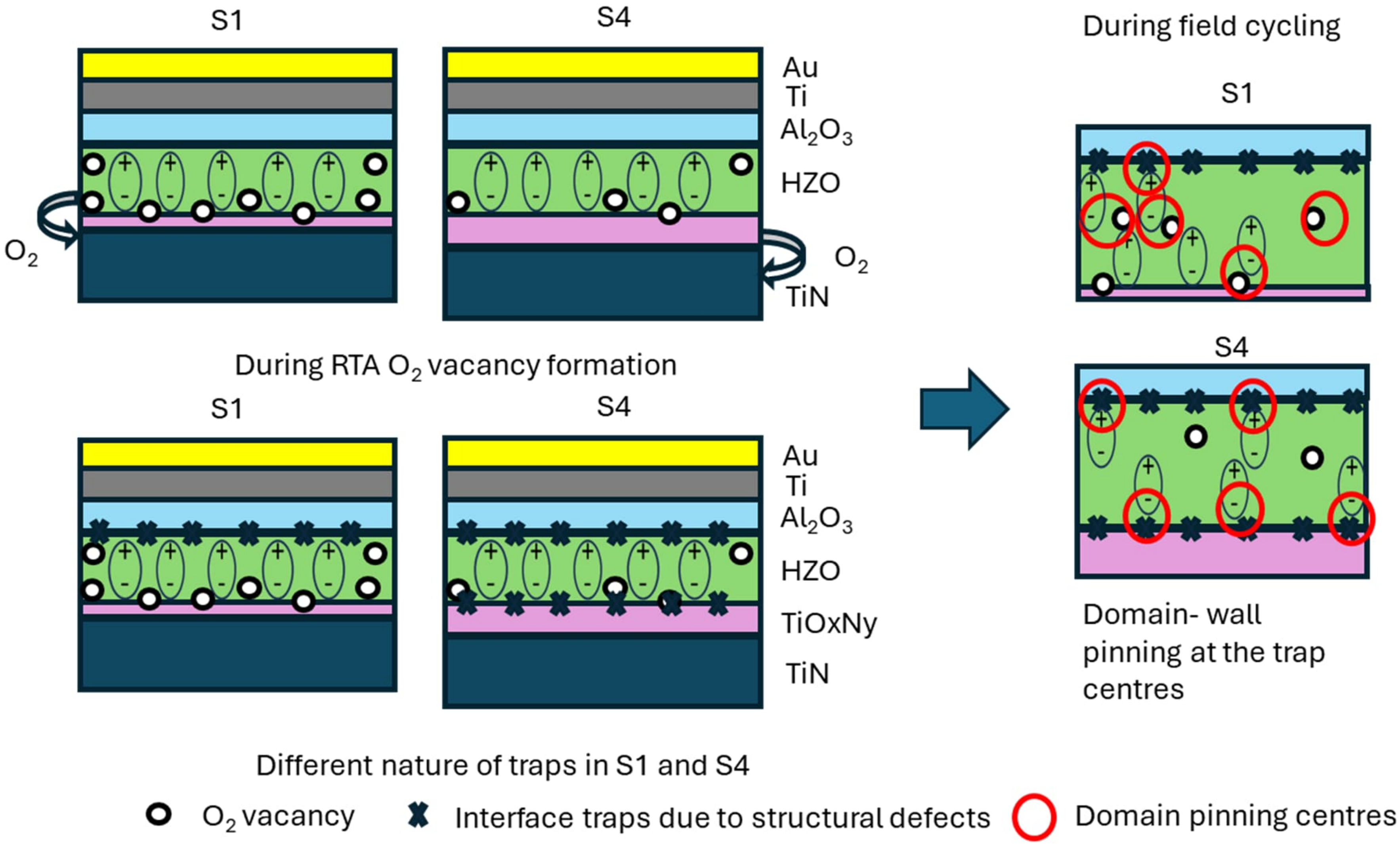
P. Srivari et al., IEEE-IIRW 2025 (accepted, to be published in IEEE X'Plore).

HZO thin film capacitors – fatigue and recovery



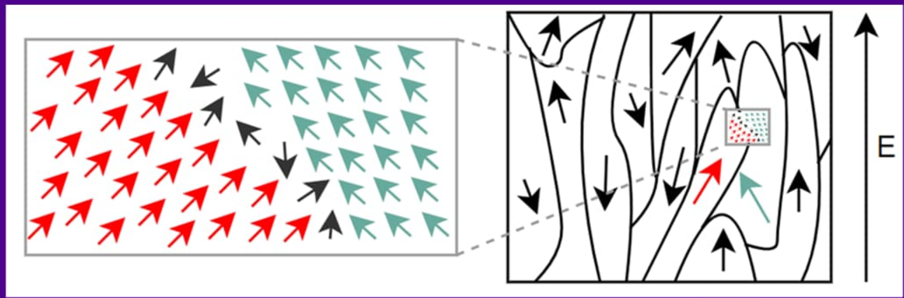
X. Li, P. Srivari, S Majumdar; Nanoscale 17, 6058 – 6071 (2025).

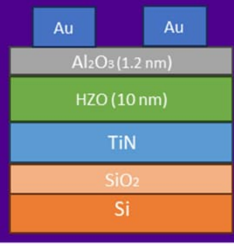
HZO fatigue and recovery– role of interface



X. Li, P. Srivari, S Majumdar; Nanoscale 17, 6058 – 6071 (2025).

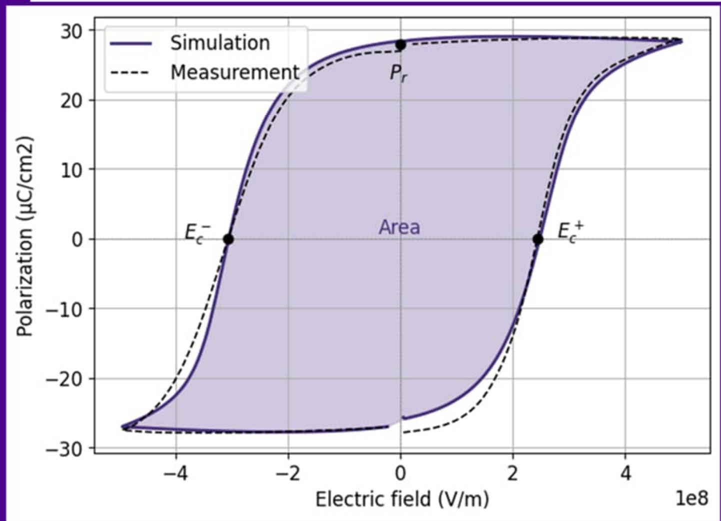
HZO thin film capacitors – Jiles- Atherton Model

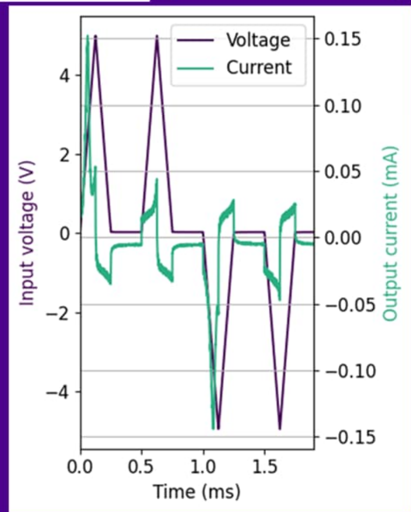




Algorithm to solve polarization time development

1. $D(t) = P_{\text{irr}}(t - \Delta t) + \epsilon_0 E(t)$
2. $D_{\text{eff}}(t) = D(t) + \alpha P_{\text{irr}}(t - \Delta t)$
3. $\frac{dD}{dt}(t) = \frac{D(t) - D(t-\Delta t)}{dt}$
4. $P_{\text{anh}}(t) = P_s\left[\coth\left(\frac{D_{\text{eff}}(t)}{a}\right) - \frac{a}{D_{\text{eff}}(t)}\right]$
5. $\delta = \text{sign}\left(\frac{dD}{dt}(t)\right)$
6. $dP_{\text{irr}} = \frac{P_{\text{anh}} - P_{\text{irr}}}{\delta k - \alpha(P_{\text{anh}} - P_{\text{irr}})} dD$
7. $P_{\text{irr}}(t) = P_{\text{irr}}(t - \Delta t) + \frac{dP_{\text{irr}}}{dt}(t)$
8. $P(t) = (1 - c)P_{\text{irr}} + cP_{\text{anh}}$





E. Paasio, M. Prunnila, S. Majumdar, https://ieeexplore.ieee.org/abstract/document/10254398
E. Paasio, R. Ranta, S. Majumdar, Adv. Electron. Mater. 11(9), 2400840 (2025)

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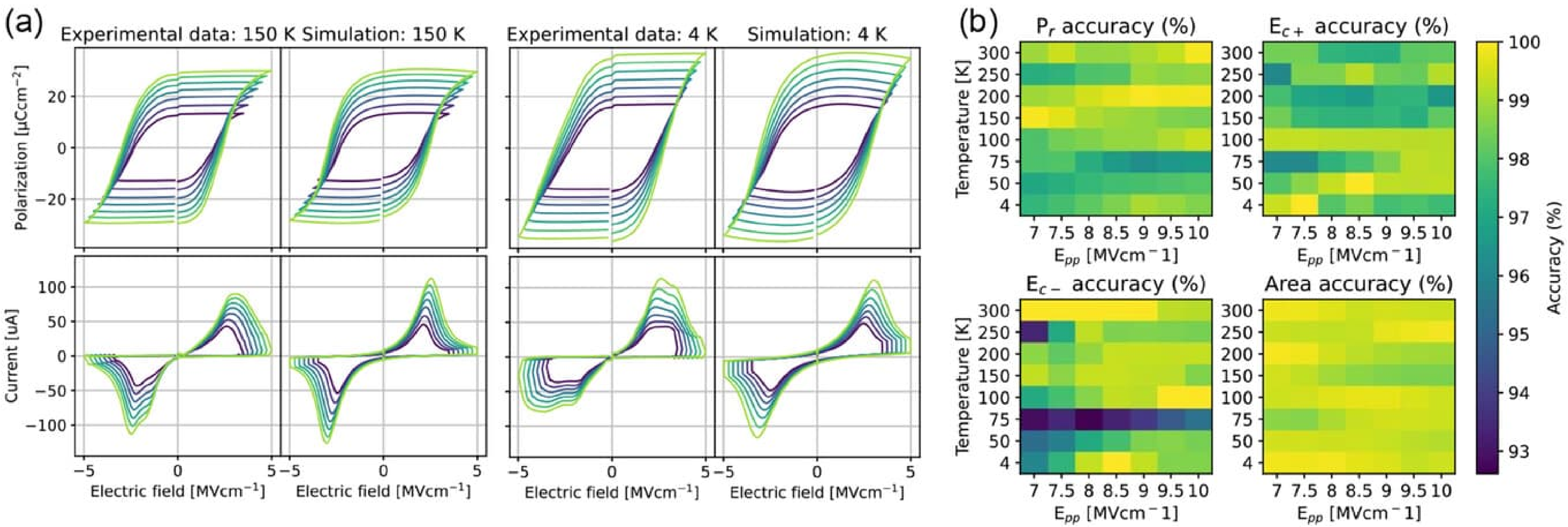
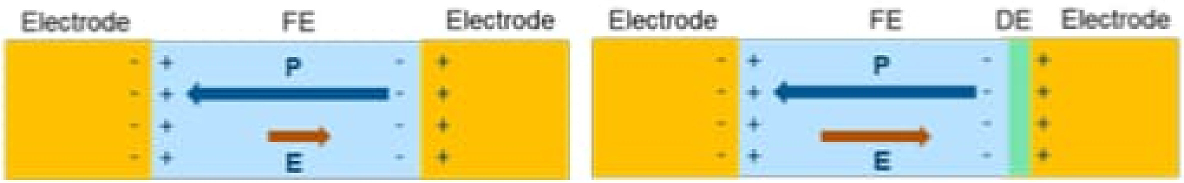
HZO thin film capacitors – Jiles- Atherton Model

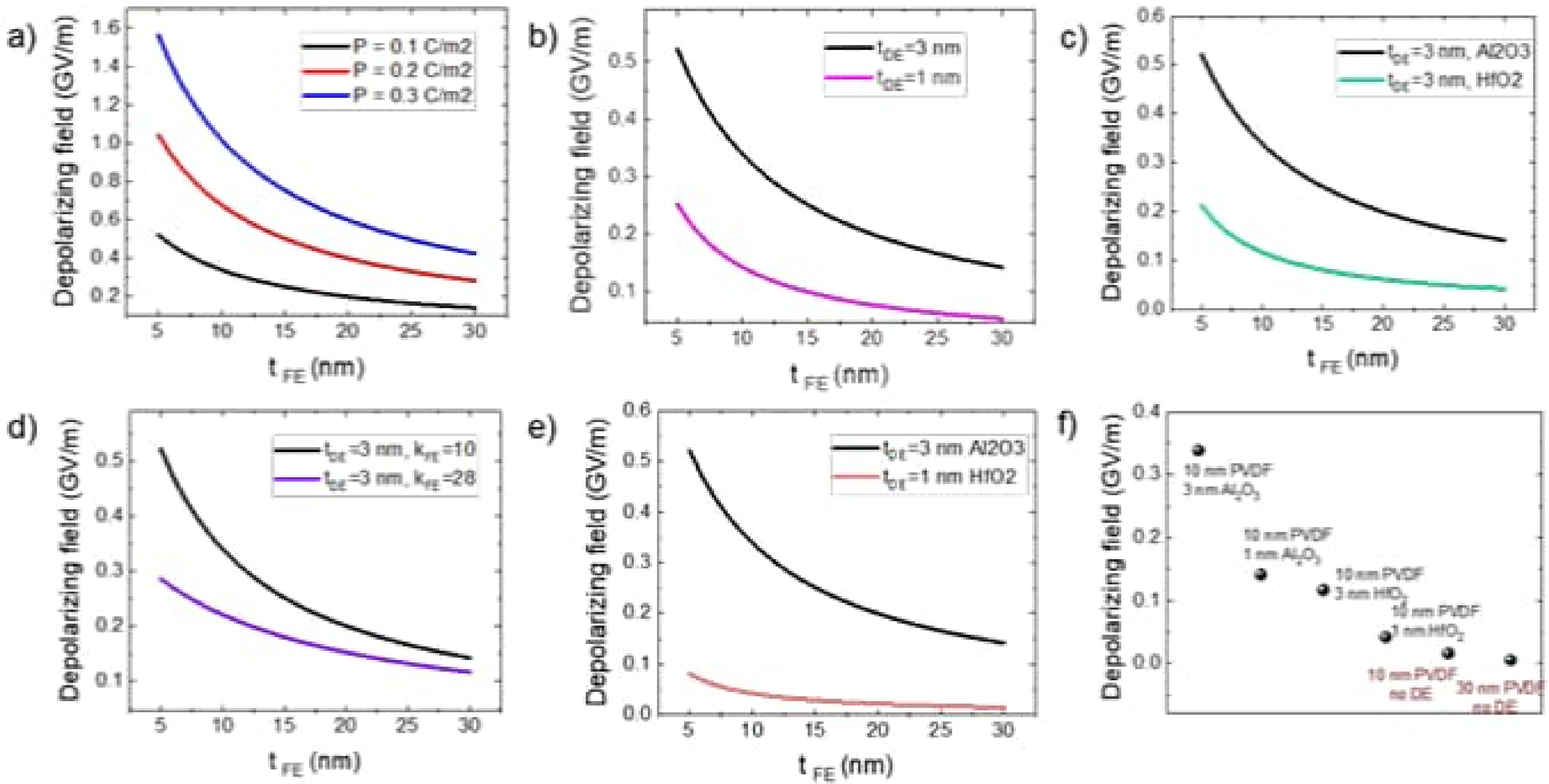


E. Paasio, R. Ranta, S. Majumdar, Adv. Electron. Mater. 11(9), 2400840 (2025)

Multiple time constants using engineered depolarization fields

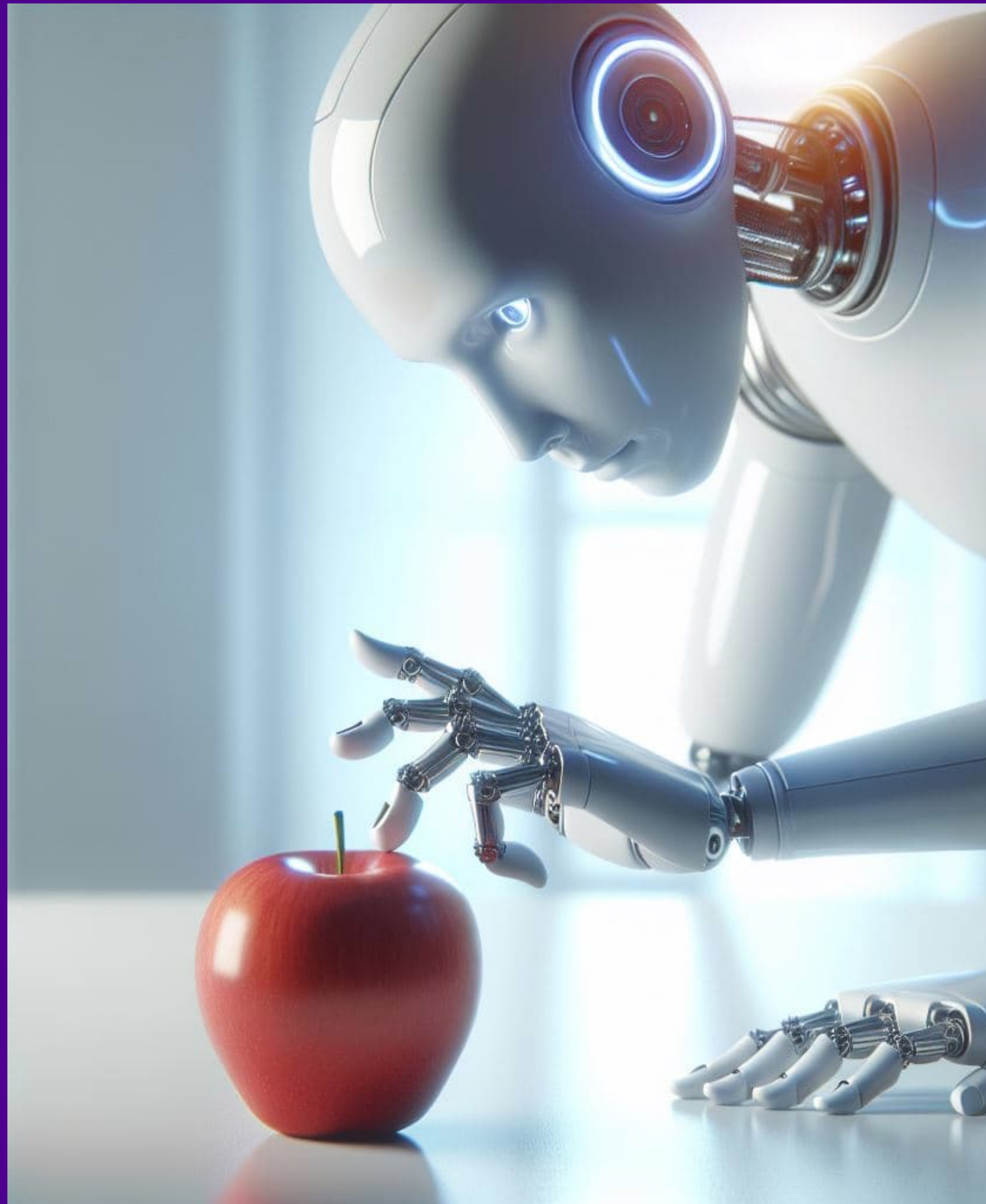
S5. Effect of interfacial oxide layer of the gate stack on the ferroelectric depolarization field



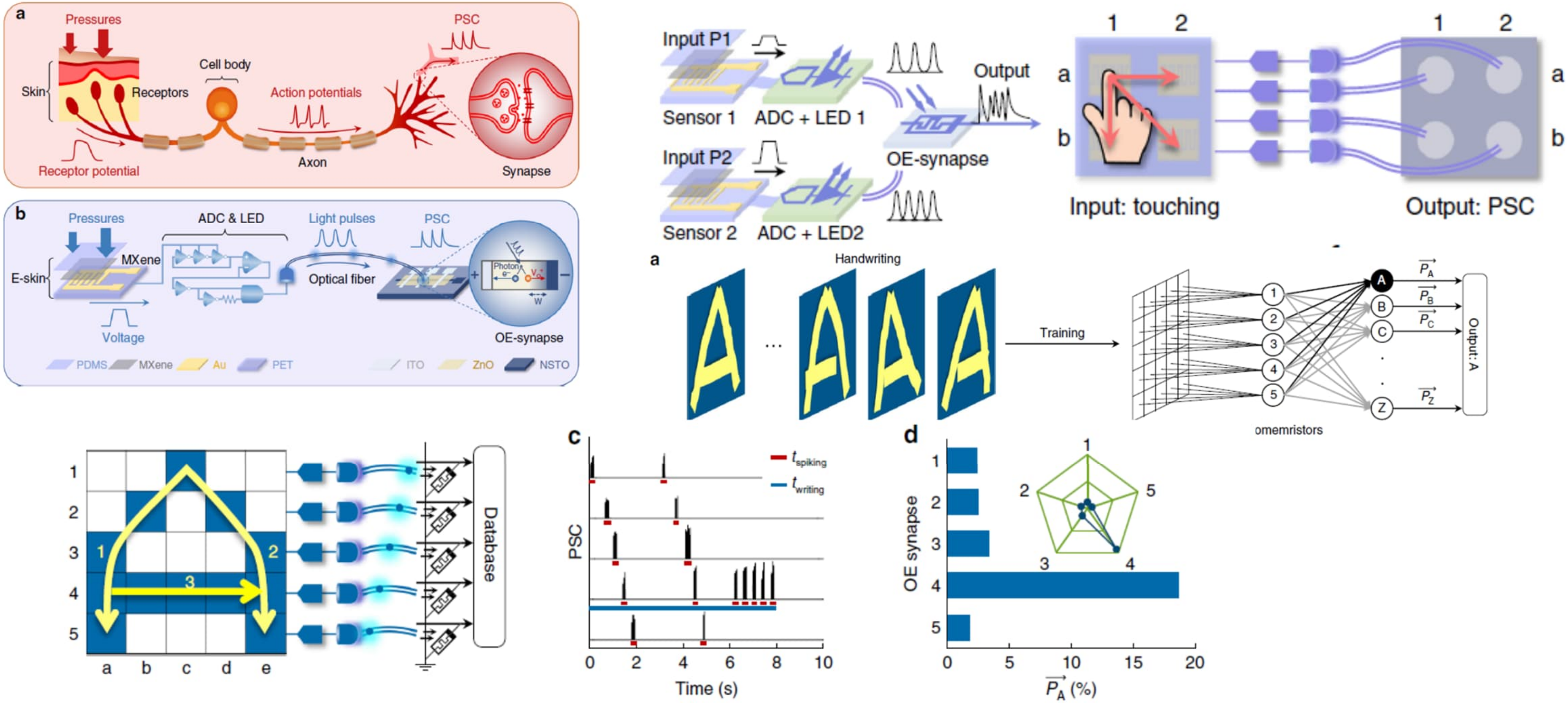


S. Majumdar *et al., Advanced Intelligent Systems 5 (11), 2300391 (2023)*

Sensors with computing

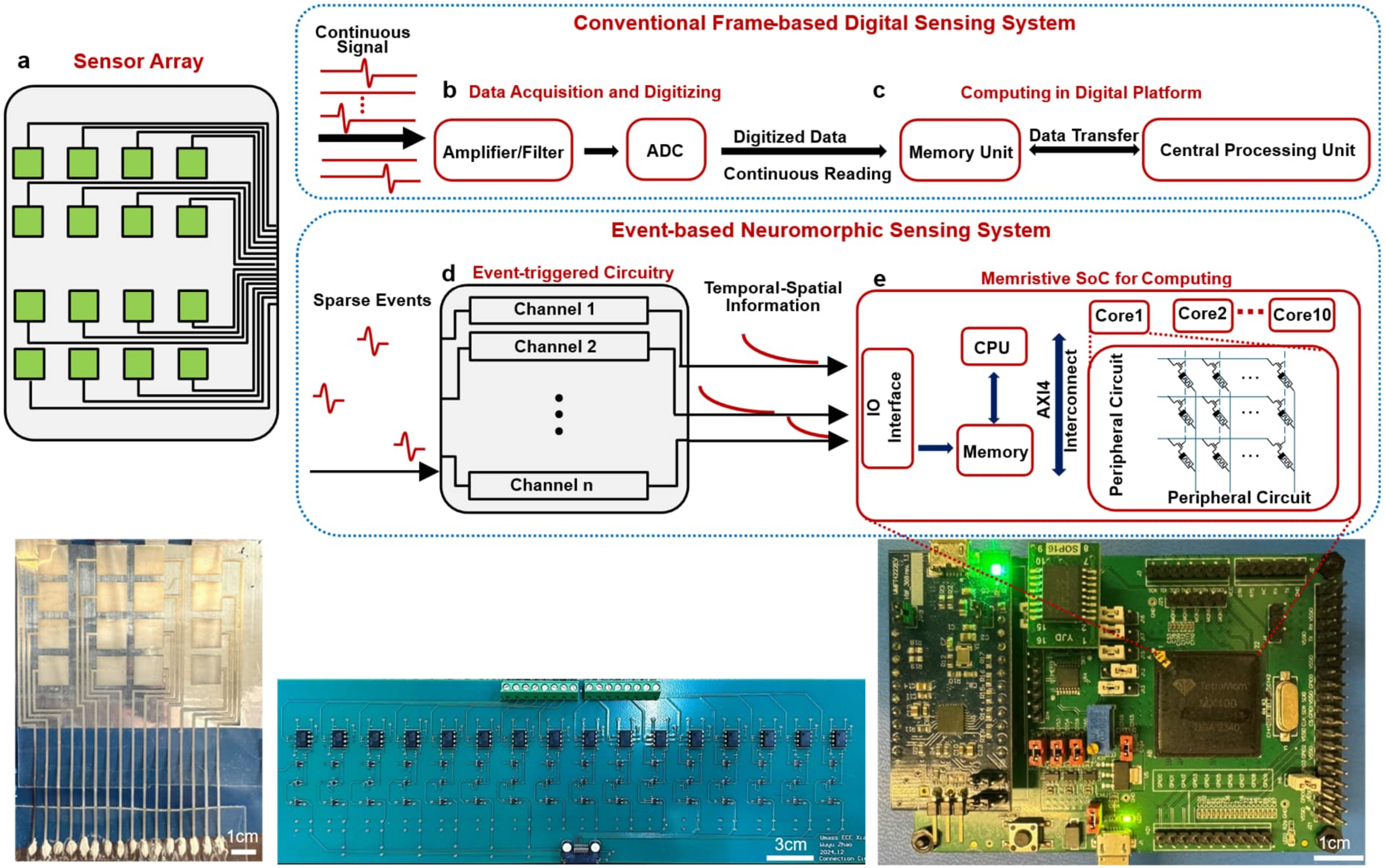


Near-Sensor Computing



Tactile sensory coding and learning with bio-inspired optoelectronic spiking afferent nerves. Nature communications 11 (1), 1-9 (2020).

Near-Sensor Computing



Event-based neuromorphic sensing system with flexible haptic sensors and a memristive system on a chip
W Zhao, S. Majumdar et al., Nature Sensors 1, 163 – 171 (2026).

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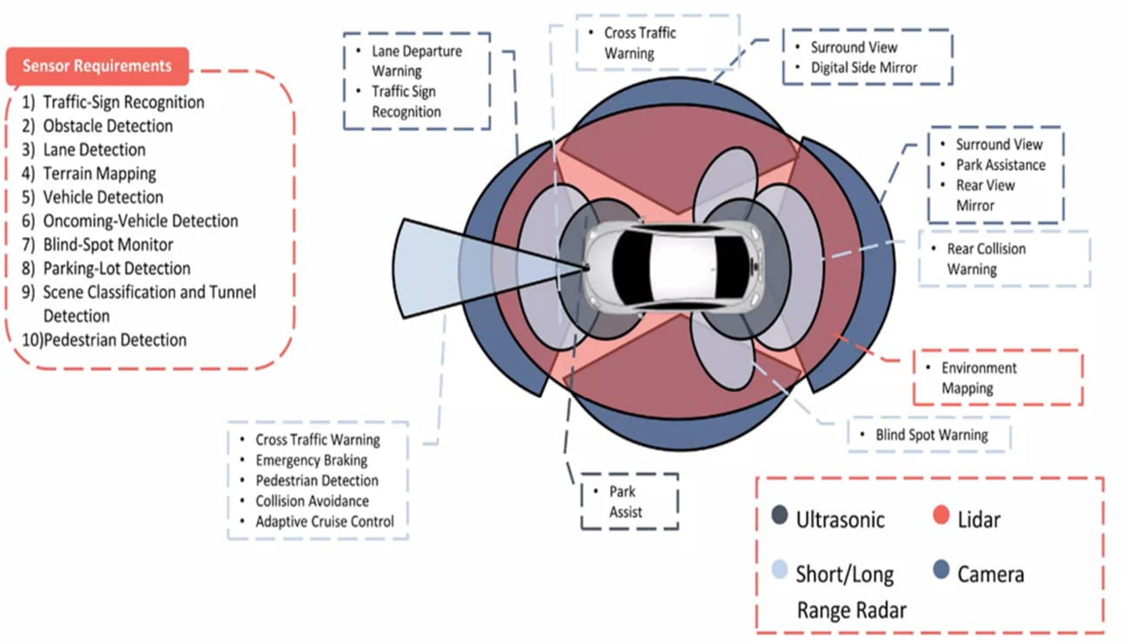
Memristive Associative Learning in Autonomous Cars

•In an autonomous vehicle, multiple sensors work together to provide comprehensive environmental awareness and safety for the vehicle in various driving situations. This arrangement allows the autonomous vehicle to effectively perceive and respond to complex, real-world scenarios.



The vehicle surrounded by various sensor types:

•**Ultrasonic** (gray),
•**Lidar** (red),
•**Short/Long Range Radar** (blue),
•**Camera** (light blue).

The sensor areas are linked to specific functionalities such as:

•Lane departure warning,
•Cross-traffic warning,
•Emergency braking,
•Collision avoidance,
•Pedestrian detection,
•Adaptive cruise control,
•Park assistance,
•Surround view, and more.

•Associative learning can make the car take right decision in absence of failure or malfunctioning of some sensor systems.

Bhardwaj, K., D. Semenov, R. Sotner, and S. Majumdar, “A Memristive Associative Learning Circuit for Fault-Tolerant Multisensor Fusion in Autonomous Vehicles,” Advanced Intelligent Systems 8 (2025): 2500215.

K. Bhardwaj, D. Semenov, R. Sotner and S. Majumdar, "Preventing False Activations in Autonomous Vehicles: A Memristive Associative Learning Approach with Selective Sensor Pairing," *2025 14th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Dresden, Germany, 2025, pp. 1-4, doi: 10.1109/MOCAST65744.2025.11083932.

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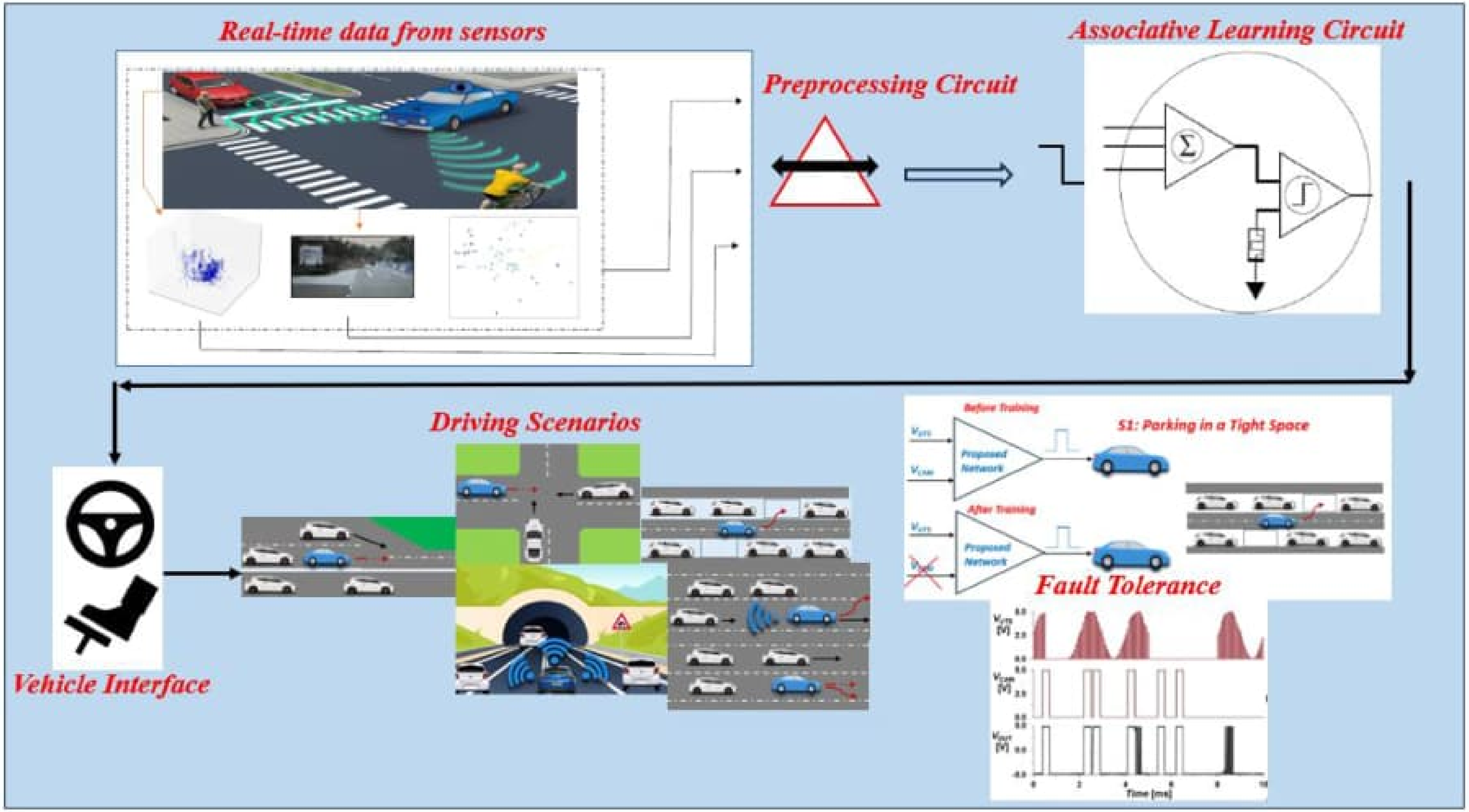
Sensor Fusion and Associative Learning in Autonomous Cars



Bhardwaj, K., D. Semenov, R. Sotner, and S. Majumdar, “A Memristive Associative Learning Circuit for Fault-Tolerant Multisensor Fusion in Autonomous Vehicles,” Advanced Intelligent Systems 8 (2025): 2500215.

A. D. Arkalgud, I. Arora, K. Bhardwaj and S. Majumdar, "Real-World Data-Driven Fault-Tolerant Multimodal Sensor Fusion with Neuromorphic Associative Learning Circuit," 2025 IEEE 7th International Conference on Emerging Electronics (ICEE), Bengaluru, India, 2025, pp. 1-4, doi: 10.1109/ICEE67165.2025.11409959.

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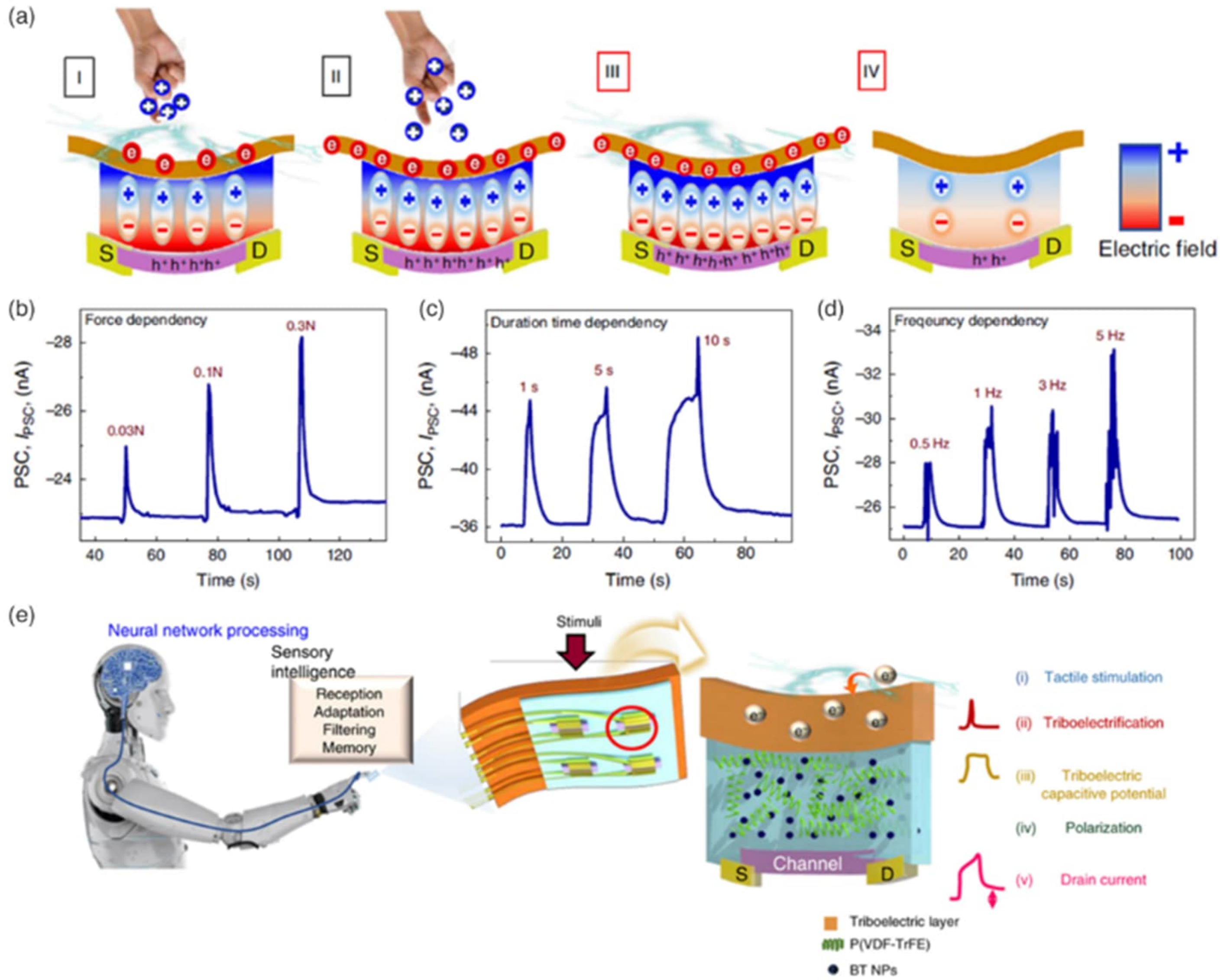
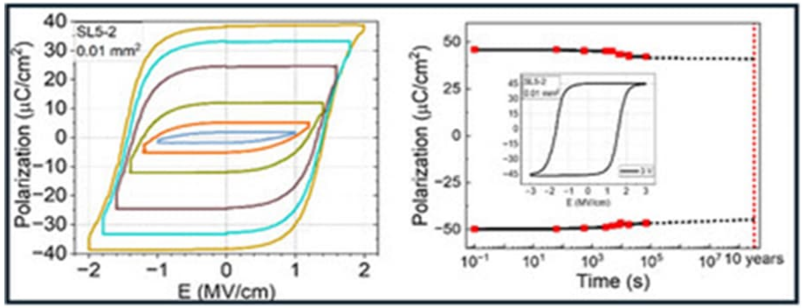
Future work: Towards In-Sensor Data Processing

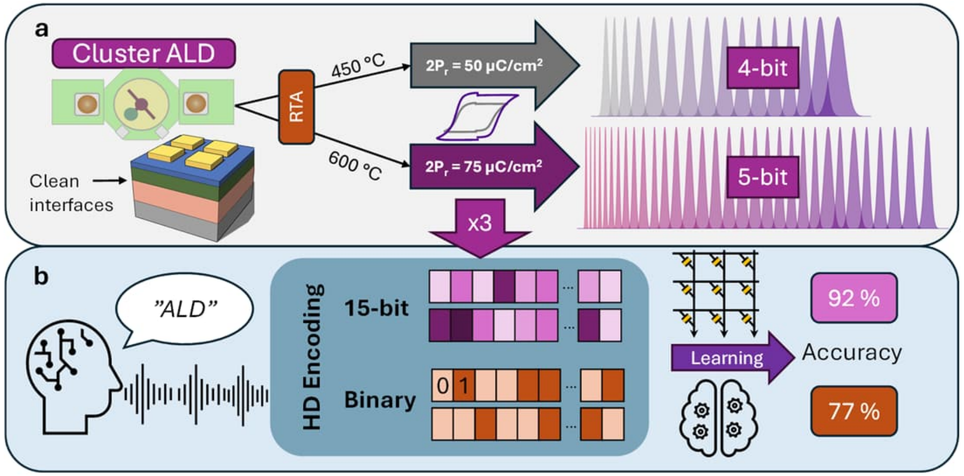


Back-End CMOS Compatible and Flexible Ferroelectric Memories for Neuromorphic Computing and Adaptive Sensing, S. Majumdar, Advanced Intelligent Systems, 4, 2100175 (2022).

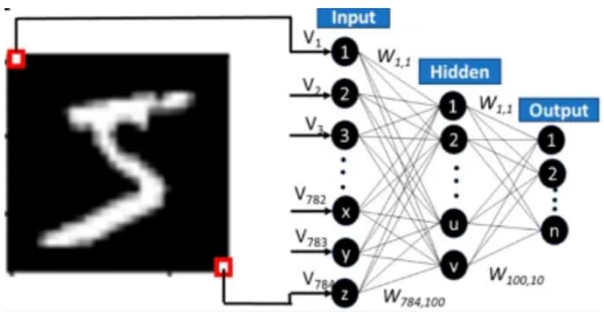
Conclusion



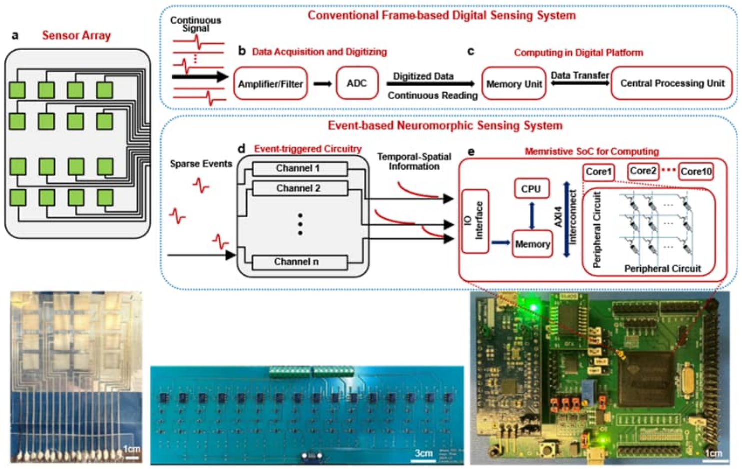
Low operating voltage NVM



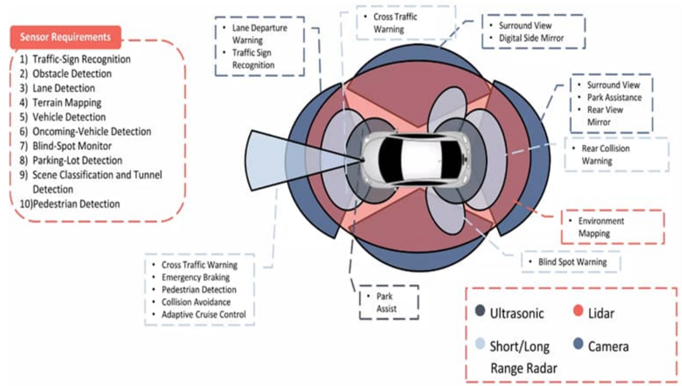
Capacitive IMC and HDC



Resisitive IMC

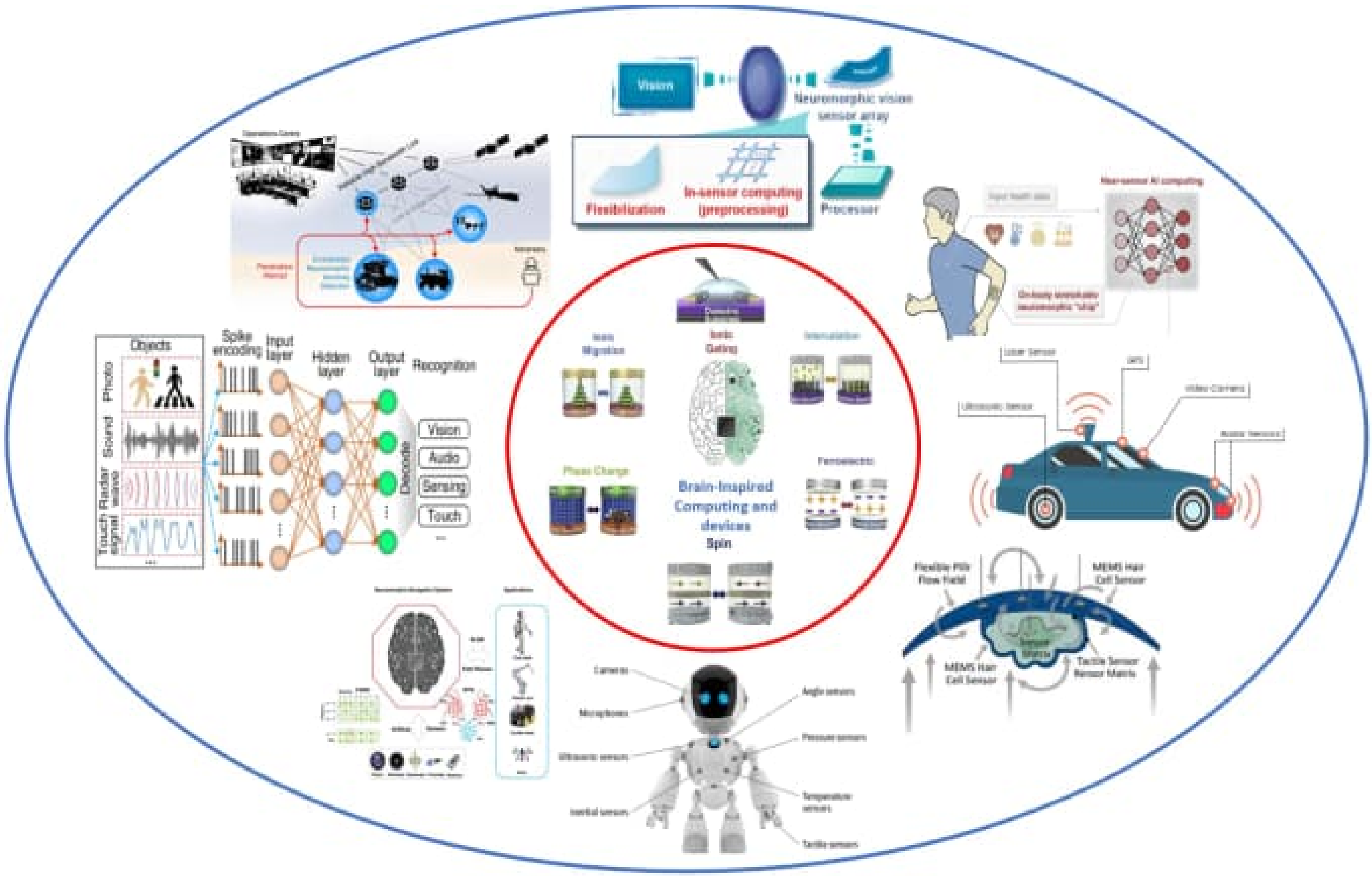


Near - sensor Computing



Sensor Fusion and decision making at the Edge

Intelligence everywhere will not be possible without a HW revolution and HW-SW co-optimization



Neuromorphic Electronics for Intelligence Everywhere: Emerging Devices, Flexible Platforms, and Scalable System Architectures , K. Bhardwaj, S. Majumdar et al., Adv. Mater. (Accepted Manuscript, 2026).

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Relevant publications

S. Majumdar et al.:

- *Adv. Mater.* 2016, *28*, 6852
- *Adv. Funct. Mater.* 2018, *28*, 1703273
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- *APL Mater.* 2019, 7, 091114
- *Adv. Intell. Syst.* 2019, 1, 1900036
- *Nature Commun.* 2020, 11 (1), 1-9
- *Nanoscale* 2021, 13, 11270
- *Adv. Intell. Syst.* 2022, 4, 2100175
- *Adv. Mater.* 2022, 34, 2201248
- *Neur. Comp. Eng.* 2022, 2, 041001
- *Adv. Intell. Syst., 5 (11), 2300391, 2023.*
- *npj 2D Mater. Appl.* 7, 18, 2023.
- *Adv. Elec. Mater, 10, 2300879,* 2024.
- *Frontiers in Nanotechnology, 6, 1-26*, 2024.
- *Nanoscale 17, 6058 – 6071, 2025.*
- *Adv. Elec. Mater, 11, 2400840, 2025.*
- *APL Machine Learning, 3, 020902, 2025.*
- *Adv. Intell. Syst, 2500215, 2025 .*
- *Mater. Sc. Semicond. Proc. , 2026 (in review),* [*https://arxiv.org/abs/2412.11288*](https://arxiv.org/abs/2412.11288)
- *Adv. Mater. Tech., e02027, 2026.*
- *Adv. Mater, 2026 (in press).*
- *Nature Microsys. And Nanoeng. 2026 (in review).*
- *Nature Sensors, 1, 163–171, 2026.*

Acknowledgements

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